RF Reference Generation for the Ground Test Accelerator*

Amy H. Regan and Peter M. Denney
MS-H827, Los Alamos National Laboratory, Los Alamos, NM 87545

Abstract

This paper describes the implementation plan for the radio-frequency (rf) reference generation subsystem of the Ground Test Accelerator (GTA). The master oscillator and most of the required components of this subsystem have been acquired and tested. Hardware descriptions and test results are cited when available. Each GTA control subsystem requires a coherent, phase-stable signal from the rf reference generation subsystem to regulate the rf field in its corresponding cavity of the accelerator. The rf reference generation subsystem is configured in a star-distribution format, originating at a master oscillator that supplies three phase-coherent frequencies harmonically related to a fixed fundamental. Phase-locked loops and Wilkinson splitters distribute these signals to many different output ports. VXI monitoring modules measure the stability of the signals being distributed. Any shift in phase of the rf reference signals from the reference generation subsystem to each cavity-control subsystem will translate directly into phase errors between cavities. The allowed tolerance on the phase error for the reference signals is +/- 0.15 degrees.

I. Subsystem Description

The rf system of the GTA operates at three harmonically-related frequencies: 425 MHz, 850 MHz, and 1700 MHz. Configured in a star-distribution network, shown in Figure 1, the rf reference generation subsystem provides coherent, phase-stable signals to each cavity field-control subsystem of the GTA. The rf transport mechanism for this network has been addressed in another report [1] and will not be covered in this paper except to note that the tested rf transport subsystem holds the phase error through 150 feet of phase-stable cables to +/- 0.036 degrees, thus allowing a +/- 0.114-degree phase error budget for the rf reference generation subsystem.

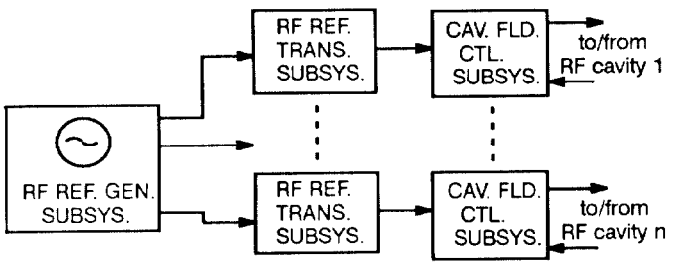

Figure 1. RF Reference Distribution Network

The master oscillator generates three fixed-frequency signals that are harmonically related to a fundamental. Each output is divided a number of times and distributed to individual cavity field-control subsystems. Figure 2 illustrates a functional block diagram of the rf reference generation subsystem.

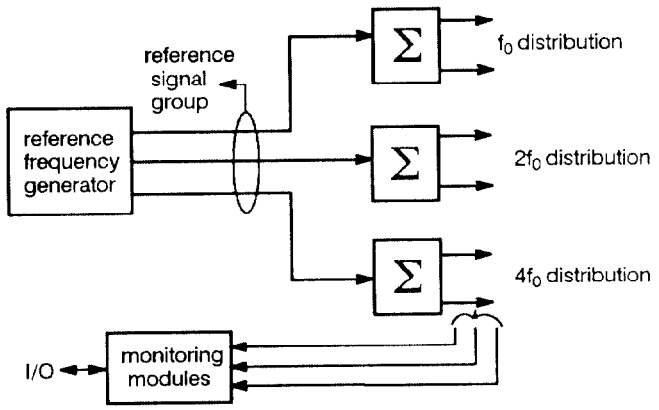

Figure 2. Functional Block Diagram of RF Reference Generation Subsystem

The rf reference generation subsystem design is based on modularity: simply by changing a few frequency-dependent components, the higher frequencies' architecture is the same as the fundamental's. The distribution requirements for the three frequencies differ such that a small number of cavities are driven at f_0 and $4f_0$ while most operate at $2f_0$. To maintain the modularity of the entire subsystem, however, each frequency leg was designed in a similar fashion with the number of outputs differing only by a binary factor. A phase-locked loop governs the phase stability of the output signals of the distribution stage relative to the input signal from the master oscillator. Figure 3 is a block diagram of the $2f_0$ leg of the rf reference generation subsystem.

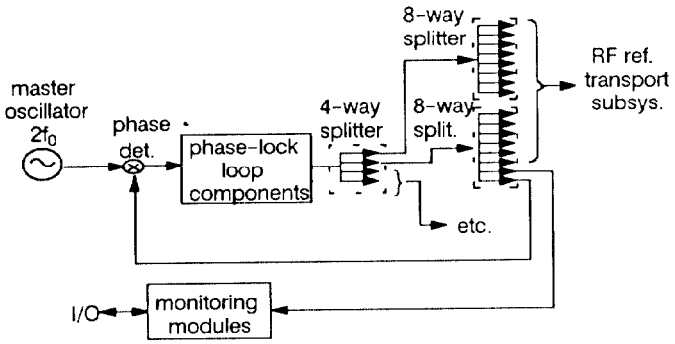

Figure 3. Block Diagram of $2f_0$ Leg

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II. Hardware Descriptions and Test Data

A. Master Oscillator

The master oscillator of the subsystem is a specially ordered continuous-wave model from Techtrol Cyclonetics, Inc. This frequency generator is a 19" rack-mount unit that utilizes an 8.5-MHz crystal as its standard. Its specifications include three internally locked, harmonically related, fixed-output frequencies (the fundamental being 425 MHz +/- 1 kHz) with a long-term frequency stability of 1×10^{-9} per day and short-term stability of 5×10^{-12} per second. The master oscillator's measured performance is presented in Table 1.

Table 1. Master Oscillator Performance

Fundamental Performance

Frequency (Hz)	425,000.0	850,000.0	1,700,000.0
Power out (dBm)	+15.0	+14.6	+15.1
Harmonics (dBc)	-44	-50	-60
Sub-har. (dBc)	<-60	<-60	-54
Spurious (dBc)	<-70	<-70	<-70

Single-Sideband (SSB) Phase Noise to Carrier Ratio (dBc/Hz)

Offset \ Freq	425 MHz	850 MHz	1700 MHz
10 Hz	-87	-81	-72
100 Hz	-107	-99	-90
1000 Hz	-128	-121	-113

B. Phase-Locked Loop

The output power of the final splitter stage must be +20 dBm, which means an amplifier is needed to boost each master oscillator output signal before the signal is distributed to a large number of outputs. Because the amplifier will inherently degrade the phase stability of the signal, a feedback circuit in the form of a phase-locked loop (PLL) must be incorporated to preserve phase integrity at the splitter outputs. Figure 4 depicts the phase-locked loop for the f_0 portion of the rf reference generation subsystem.

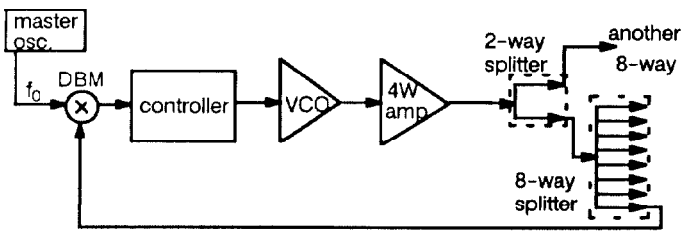

Figure 4. Phase-Locked Loop Block Diagram

The phase-locked loop incorporates a double-balanced mixer (DBM) as the phase detector, a loop controller, a voltage-controlled oscillator (VCO), a 4-watt amplifier, and Wilkinson power splitters. Each component was selected in order to minimize the phase noise of the output signal. The first component to be investigated was the VCO. A PLL is effectively a low-pass filter with respect to the phase noise of the reference signal and a high-pass filter with respect to the phase noise of the VCO [2]. The cutoff frequency in both cases is the loop bandwidth. Hence, if the phase noise specifications of the reference signal are known, a VCO is selected and the loop bandwidth chosen to provide optimum phase noise at the output of the PLL. Figure 5 illustrates the SSB phase noise specifications of the master oscillator and the varactor-tuned VCO chosen for this design. Clearly, the optimum loop bandwidth is 250 kHz.

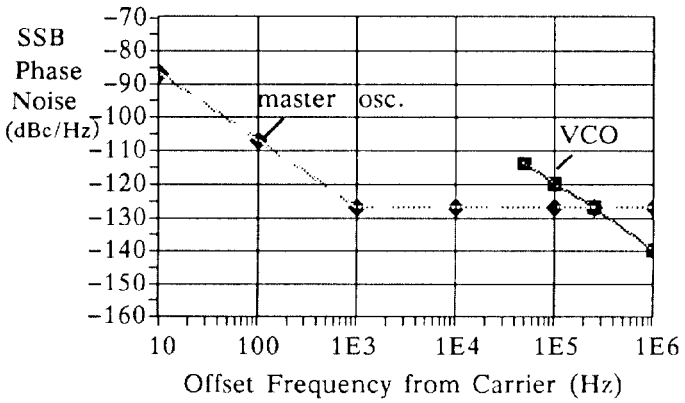

Figure 5. Phase Noise of Master Oscillator and VCO

Short-term phase jitter of the PLL output signal can be estimated from the data in Figure 5 and the following equation. [3]

$$\phi^2 = \int_{f_1}^{f_2} \frac{2N_{op}}{C} df$$

where $\phi \equiv$ phase jitter,
$N_{op} \equiv$ phase noise power density,
$C \equiv$ carrier signal power,
and $f_1 = 10$ Hz and $f_2 = 1$ MHz.

The lower frequency limit was chosen to be 10 Hz because the beam pulse in the accelerator operates near this frequency; therefore, phase changes occurring at lower frequencies can be considered long-term phase jitter. The upper frequency limit was chosen to be 1 MHz because the cavity field-control subsystem operates within a 1-MHz bandwidth. The PLL phase jitter was approximated by considering only the noise contribution of the master oscillator below 250 kHz and then adding the noise contribution of the VCO above 250 kHz. The short-term phase jitter was estimated to be 3.3×10^{-4} degrees. Obviously, noise contributions from other components within the PLL will increase the phase jitter of the output signal. The 4-watt amplifier, for example, will add to the phase noise of the VCO by an amount equal to the amplifier noise figure. This added noise will transfer to the output signal at frequencies above the loop bandwidth. On the other hand, the noise floor generated by the phase

detector and the controller will transfer to the output signal at frequencies below the loop bandwidth. For this design, a mixer and an operational amplifier have been selected that will ensure a noise floor below -128 dBc/Hz.

Long-term phase stability of the output signal is of equal importance and highly dependent on the temperature stability of the loop components. The DBM, the controller, and the splitters are the major contributors to long-term phase jitter. Because the dc offset drift of the DBM translates directly to phase error, a mixer with negligible offset drift is used. Operational amplifiers in the controller produce an input noise voltage that drifts with respect to temperature. This change in dc input voltage also translates to phase error; for this reason, low-noise operational amplifiers with good temperature stability are utilized. For additional safeguards, the circuit board containing the DBM, controller, and VCO is temperature regulated.

Once all of the components were selected and the transfer functions determined, the controller was designed using Bode analysis. A lag-lead compensator was chosen, with an integrator providing the lag compensation. The integrator ensures maximum dc gain in order to minimize long-term phase errors caused by dc drifts in the VCO. Lead compensation was used to ensure stability of the PLL. The gain of the controller was adjusted to provide a loop bandwidth of 250 kHz.

C. Splitters

The overall design of the subsystem relies strongly on the phase stability of the Wilkinson splitters. The assumption is that the phase of all of the output ports will remain constant if one output port is held constant by the phase-locked loop. Each splitter is formed by one or more stages of Wilkinson dividers designed in microstrip for application on RT/duroid 6002 dielectric. RT/duroid 6002 was chosen because of its tight permittivity tolerance and its permittivity stability with respect to temperature. Because permittivity and insertion phase are directly proportional, a stable dielectric permittivity value with respect to temperature assures stable insertion phase. Temperature chamber data of Wilkinson splitters indicate that the phase change of individual outputs relative to each other that is due to temperature changes in the 25 to 40 degree C range is negligible. For added insurance, however, all of the splitters associated with a particular phase-locked loop are mounted together on an aluminum block, creating a large thermal mass. Hence, a negligible thermal gradient is maintained.

D. Monitoring Modules

The rf reference signals are monitored through off-the-shelf VXI instruments. A power meter monitors the level of the signals out of the last stage of splitters, while a frequency counter with nine-digit resolution records the output frequency. The frequency counter uses as its reference a rubidium standard which, with a long-term stability less than 5×10^{-11}/month, is more stable than the master oscillator. Using this extremely stable external standard for the frequency counter allows the phase-locked loop output signal to be properly monitored.

In addition to these modules, two switching modules are required in order to select the various frequencies, and a custom-built phase-lock indicator module provides an interrupt should any of the phase-locked loops lose lock. All of these modules are message-based devices and are housed in a separate VXI crate in the rf reference rack.

III. SUMMARY

The rf reference generation subsystem for the GTA has been designed and individual components have been tested. The master oscillator has been delivered to Los Alamos and in-house test results have been favorable.The phase-locked loop has been designed to minimize short-term, as well as long-term, phase jitter in order to stay within the combined phase error budget of 0.114 degrees. A prototype phase-locked loop has been built and testing is currently in process. Final development of the rf reference generation subsystem is ongoing with an anticipated operational date in June 1991.

IV. ACKNOWLEDGEMENTS

The rf reference rack is a product of a team effort. The following people are recognized for their considerable contributions: M.Curtin, S. Jachim, R. Przeklasa, and A. Young.

V. REFERENCES

[1] S.P. Jachim, A.H. Regan, W.D. Gutscher, E.F. Natter, M.T. Curtin, P.M. Denney, "A Phase-Stable Transport System," *Proceedings Neutral Particle Beam Technical Symposium*, San Diego, CA, May 1990.

[2] V. Mannassewitsch, *Frequency Synthesizers: Theory and Design*, New York: John Wiley & Sons, 1987, pp. 24-27.

[3] W.P. Robins, *Phase Noise in Signal Sources (Theory and Applications)*, London: Peter Peregrinus Ltd., 1984, p. 153.