An Active Interlock System for the NSLS X-Ray Ring Insertion Devices

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Abstract

This paper describes the design and operation of an active interlock system which has been installed in the NSLS X-ray electron storage ring to protect the vacuum chamber from thermal damage by mis-steered high power photon beams from insertion devices (IDs). The system employs active beam position detectors to monitor beam motion in the ID straight sections and solid state logic circuitry to "dump" the stored beam in the event of a fault condition by interrupting the RF. To ensure a high degree of reliability, redundancy and continuous automatic checking has been incorporated into the design. Overall system integrity is checked periodically with beam at safe levels of beam current.

I. INTRODUCTION

The NSLS X-ray electron storage ring operates with several insertion devices (IDs) which generate high power photon beams sufficiently intense to cause severe thermal damage to the machine aluminum vacuum chamber if mis-steered. Presently, the IDs consist of two hybrid wigglers (HBW) at X-21 and X-25 and a 5 Tesla superconducting wiggler (SCW) at X-17, all located in their respective straight-sections. Power density in the X-25 HBW photon beam is of the order of 1.75 kW/mrad^2 at 250 mA. The power carried by a photon beam from an insertion device varies as $i\gamma^2K^2$, where i is the beam current, γ is the energy and K is the ID field factor. In the low beta ID straight sections, the beam may be deflected by as much as $\pm$ 8 mrad and still survive in the machine. Due to various reasons it was not possible to design the X-ray ring vacuum chamber to be safe under all possible operating conditions, however, the chamber is safe for $i < 7.0$ mA, all horizontal beam deflection angles (except in the case of the SCW) and for vertical angles $< \pm$ 2.5 mrad. Vertical deflections $> \pm$ 2.5 mrad could expose parts of the vacuum chamber to incident radiation and must be avoided.

To protect the machine chamber from damage due to mis-steered beams, an interlock system has been developed and installed in the ring. This system utilizes active beam position detectors which continuously monitor beam motion in each of the ID straight sections and logic circuitry which interrupts the RF and dumps the stored beam in the case of a fault. The time interval within which the system must respond to an out-of-range beam has been calculated for worst case to be $\approx$ 30 msec. A portion of a typical straight section vacuum chamber protected by the interlock is shown in Fig. 1.

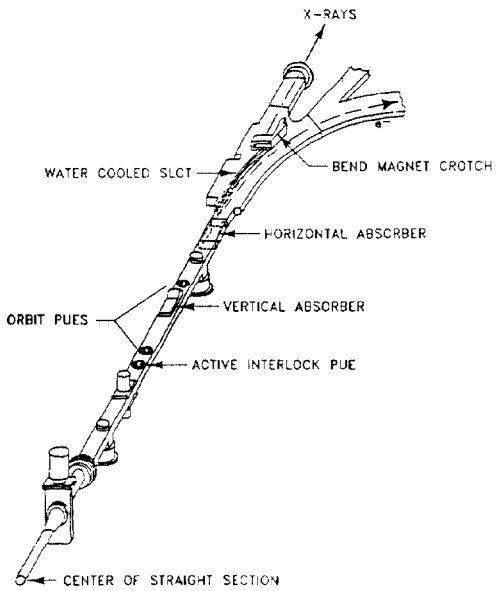

Fig. 1. Vacuum Chamber in a Straight Section

In the design of the system, various beam position monitors have been considered, including such devices as thermal and pressure sensors, radiation monitors as well as the NSLS developed RF BPMs. After careful consideration, it was decided that the BPMs would be best suited for this application.

Reliability of the interlock is ensured by using two completely redundant channels starting from the BPMs all the way through to the low-level RF switches with all components hard-wired (i.e no software links). Each redundant circuit interrupts the low-level RF drive independently. Operation of critical system components is continuously monitored in the background by dedicated micro-computers which generate warning signals to the machine operator in case of a problem. The overall system is periodically tested with beam at safe levels of beam current using one of the main NSLS control

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computers. Test software has been written to automatically generate local orbit "bumps" and move the beam at each location until a trip level is reached and the RF is pulsed off. Such tests are routinely performed prior to normal machine fills. The software checks measured values against stored data to determine whether all criteria have been satisfied and generates a "PASS/FAIL" report at the end of the test.

II. SYSTEM DESCRIPTION

A design of an NSLS interlock prototype was described in [2]. Present system realization differs from the prototype in several aspects such as circuit topology, inhibit functions, testing philosophy, etc. The design and basic operation of the system presently installed in the machine will be described by referring to the block diagram in Fig. 2. In each of the straight sections containing an ID, vertical position of the stored beam is monitored both upstream and downstream of the device at the locations of the dedicated RF PUEs. For reliability, two BPMs are connected to each PUE, one from interlock channel "A" and the other from channel "B". The output of each BPM is monitored by a window comparator in the local logic chassis (LLC). The center of the window is set to match the offset voltage of the BPM if any, and the width of the window is adjusted for the allowable range of beam displacements at the PUE. If the comparator detects an out-of-range signal, it generates a fault bit which is transmitted to the Central Logic Chassis (CLC). After receiving a fault signal, CLC sends an interrupt request to the RF Interface Chassis (RFI) which then momentarily interrupts the low level RF drive signal to all RF systems (RF1, RF2, etc.). The RF interrupt pulse must be long enough to "dump" the beam (few milliseconds) yet short enough so as not to disturb the thermal equilibrium of the RF transmitters and accelerating cavities. The presence of beam in the machine is monitored independently by two detectors (log amps) and if the beam is present at the end of the interrupt interval, all high-level RF systems are crashed by crow-barring the plate power supplies. Response time of each interlock channel has been intentionally slowed down to approximately 20 ms to avoid false trips.

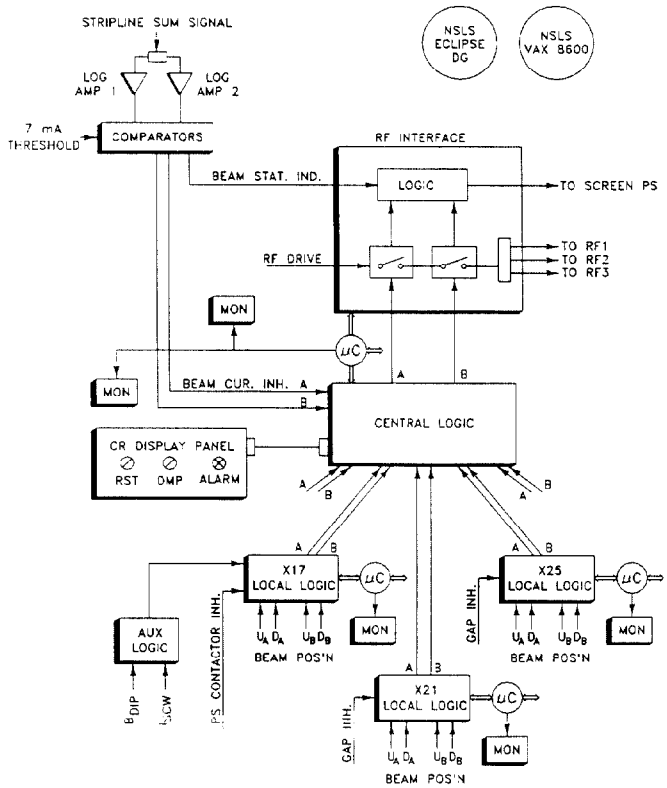

Fig. 2. System Block Diagram

Each of the local nodes as well as the central node of the system contains a dedicated micro-computer. The computer hardware consists of a Motorola VME-133 CPU, battery backed up memory, GPLS board (NSLS General Purpose Interface Board), ADC and bit I/O boards- all housed in a VME-format crate. The central node micro also services the RFI. The function of each micro is to monitor the status of latches, set control bits, perform digital filtering, perform comparison tests between redundant detectors and to generate video displays. All of the dedicated micros communicate with the main NSLS control computers via Ethernet.

The following is a description of some of the more important features of the interlock system:

First Event Latches

The LLCs and the CLC contain so-called first event latches to permit capturing of momentary window comparator fault signals. The first event latches can be made "transparent" by means of control bits which is useful in system testing.

Local and Global Inhibits

To permit testing of the individual blocks and of the overall system, local as well as global inhibits have been incorporated in the design. A local node may be automatically inhibited if either the gap of the insertion device is open or if the gap field is low. The entire system may be automatically inhibited for beam currents < 7 mA. Any of the inhibit signals may be overridden with control bits from the micro-computer to force-activate the interlock.

Fault Interrupt

Fault signals generated by comparators in the LLCs generate an interrupt to the local micro. The interrupt causes the last digitized output from each BPM prior to beam dump, which has been initiated by the interlock, to be saved in memory.

Automatic Testing

With micro-computers interfaced to the system, it is possible not only to monitor individual status bits and/or analog readbacks or to set control bits, but also to perform a whole range of automatic system tests. To ensure that all micros are alive and are performing the background comparison tests, "heartbeat" signals from the local and central micros are monitored by the LLCs and the CLC.

Status Display

The state of the interlock, status of the latches, inhibits and background faults are displayed on a display panel in the control room which is directly connected to the CLC. In addition to display lights, the panel contains two manual switches and a sonic alarm. One of the switches resets all latches (global reset) and the other dumps the beam. In addition to the display panel, a video monitor is used to display the overall status of the system including the RFI, the log amp detectors and the beam current transformer. The video display is generated by the central micro.

III. SYSTEM SOFTWARE

Software developed for the interlock system may be divided into the following three groups:

Local Micro Software (LMSoft)

LMSoft continuously monitors gap status bits, status of latches as well as the analog outputs of BPMs. It continuously compares BPM outputs in the A and B channels and generates background fault bits in case of a disagreement. This software also generates the gap inhibit override bits and the interlock branch test bits.

Central Micro Software (CMSoft)

CMSoft continuously monitors the status of the A and B latches in the CLC, status of the RFI latches, background fault and gap status from each local node as well as the analog outputs from the log amps and the ring current DCCT. It compares the analog signals and generates background faults, generates global current inhibit override and beam dump command bits and measures the time delay from beam dump command to actual beam dump.

Host Computer Software (HCSoft)

HCSoft includes programs for measuring BPM output/orbit bump input transfer functions, and for measuring BPM gains and offsets. It also includes the pre-fill test programs to test the interlock system prior to each regular high current machine fill. A program is also available to generate a fault report after a beam dump.

IV. TYPICAL OPERATION

A typical operational cycle of the X-ray ring is shown in Fig. 3. As illustrated, an automatic test is performed at low current (<7mA) prior to a normal fill for operations. This "pre-fill" test checks the status of each BPM, bumps the orbit in the ID regions to test the window comparators in the LLCs with the global low-current inhibit activated, and then overrides the global inhibit to dump the beam. If the pre-fill test, having checked all the necessary criteria generates a "PASS" report, the operator proceeds with a normal fill for operations.

At all times, each of the local micros and the central micro perform comparison tests between the A and B channels and between the log amps and the ring current DCCT. A fault in any of the background tests generates a warning to the machine operator.

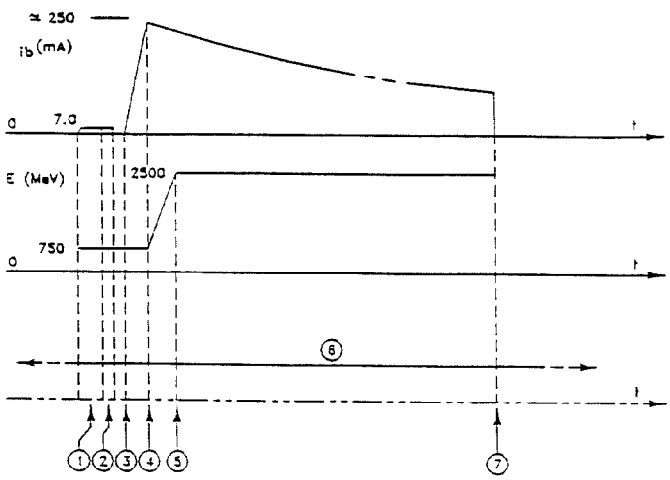

Fig. 3. A Typical Operational Cycle

V. ACKNOWLEDGEMENTS

The design of the system hardware and software evolved over a period of about a year with contributions from many individuals within NSLS as well as from other laboratories. Construction, installation and testing was performed by NSLS personnel, primarily by Jack Tallent.

VI. REFERENCES

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[2] J. Rothman and R. Nawrocky, "Active Interlock For Storage Ring Insertion Devices," *Proceedings of 1989 PAC*, IEEE Catalog No. 89CH2669-0, pp. 266-67.