

**Specialized Microprocessor Modules for
the Synchrotron Automatic Control System**
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At present a modernization of the Yerevan synchrotron control system is being performed with the aim to create multilevel architecture of computing means with the use of micro and personal computers.

To operate at the lower level, there is elaborated a set / 1-5 / of specialized modules based upon INTEL 8080 microprocessors that permit to solve the following problems :

- continuous measurement, tolerable check of parameters and formation of actions that control the accelerator subsystems;
- buffering, preliminary processing, information conversion and its transfer to a higher-level computer;
- feedback local control;

The connection of the modules with the computer is realized via the RS 232 standard interface of a "Vector" design.

The main cause for elaboration of specialized modules and rejection of using standard nuclear electronic equipment is the intention of apparatus minimization with sufficient versatility of its functional possibilities.

In the present report we consider peculiarities of the construction of the microprocessor modules elaborated and also give specifications and functional diagrams.

1. Module of Measurement and Processing of the Time Intervals /1/

The module performs measurement and preliminary processing of 50 time intervals in a fixed measurement cycle under two possible modes :

- measurement of 50 time intervals with beginning at the same moment and

termination at the different time moments in one cycle of measurements;

measurement of 16 time intervals with beginning and termination at arbitrary time moments in one cycle of measurements.

The module diagram is given in Fig.1 where the following main units are shown:

- central processor (CPU) based upon a INTEL 8080 microprocessor;
- ROM and RAM with 2 Kb each;
- RS 232 communication line adapter based upon INTEL 8251A chip which performs the connection of the module with the central computer in asynchronous mode of information exchange;
- control and synchronization circuit (CSC);
- array of counters (AC) based upon INTEL 8253 timer chips.

The accuracy of measurement of time intervals is $0.5 \mu s$, the maximum duration of the measurement cycle interval is 32 ms.

The given module is used for measuring, check and diagnosis of the driving magnetic field and basic synchronization pulses of the Yerevan synchrotron.

2. Timer Module /2/

The Timer Module has the following functional possibilities :

- programmed distribution of the basic synchronization pulse in different channels depending on the operator-preset succession;
- formation of controllable delay in fixed channels;

time selection of the basic synchronization pulse, check of its timely arrival and travelling.

A structural diagram of the module is shown in Fig. 2.

The tolerable check unit (TCU) passes the basic synchronization pulse only in the case when it falls to the tolerable "gates" whose parameters are formed by user's program.

In the commutation channel code memory (CCCM) the processor records the succession of channels' numbers according to which the comparison circuit (CC) commutes the channels with each arrival of the basic synchronization pulse. The time delay former (TDF) delays pulses in two channels by values determined by user's program. The hardware of TCU and CC as well as the introduced additional memory CCCM enabled to completely release CPU from direct control over pulse distribution process and tolerable check and to use it for solving other problems if necessary.

The main specifications of the timer module are as follows :

- the number of pulse distribution channels - 8;
- the number of time delay distribution channels - 2;
- the range of programmed time delay of pulses - from 1 μ s to 32 ms;
- accuracy of delay formation - 0.5 μ s;
- the length of the pulse distribution periodicity over channels is arbitrary, up to 256.

The timer module is used for synchronization of all output devices and physical experimental equipment with the operation cycles of the synchrotron in all modes of exploitation.

3. Universal Measurement-Control Module /3/

The Universal Module (UM) has the following functional possibilities :

simultaneous measurement of the

shape of two analog signals and realization of tolerable check;

- formation of 6 pulses with controllable time delays;
- measurement and tolerable check of duration of 16 time intervals.

A structural diagram of the UM is given in Fig. 3. Here CSC is a control-and-synchronization circuit for the array of counters AC; ADC1 and ADC2 are 10-bit analog-digital converters for the measurement of values of analog signals with repeated triggering; LVM1 and LVM2 are memories for ADC1 and ADC2, respectively to store tolerable values; CC are circuits of comparison of measured and tolerable signals. The TDF timers work on arrivals of the external triggering pulse irrespective of the CPU, which permits the UM to operate simultaneously both in the tolerable check or measurement modes and in the mode of information exchange with the central computer. The number of discretization points in the measurement of analog signals is up to 256, the pitch of discretization and measurement - 55 μ s.

The UM is the basic module for all control subsystems of slow beam ejection from the Yerevan synchrotron /4/.

4. Controlable Function Generator

The Controlable Function Generator (CFG) represents a program multichannel function generator intended for formation of controlling analog signals of arbitrary shape for 6 channels. The minimum value of signal time discretization is 1 μ s, the number of programmed values of one signal is not more than 1024. The structural diagram of the CFG is presented in Fig. 4.

12-bit digital-analog converters (DAC) form program values of functions loaded by the CFG processor to the memory of values of generated curves (DTM). The control circuit (CC) provides time fixation of the shaped curves to the process, AC are address counters. The CFG is intended for formation of the modulation curve of the RF-system and

power supply control of magnetic elements of the Yerevan synchrotron output systems.

5. Check and Diagnosis Module of State Signals /5/

The Check and Diagnosis Module (CDM) is intended for cyclic detection of state signals of "on-off" type, for the establishment of the fact of absence (presence) of changes, and for execution of diagnosis by realization of logic algorithms for situation recognition according to the state signals changes.

The CDM structural diagram is given in Fig. 5. Here M is an 8-bit multiplexer, CVR is a 16-channel 8-bit multiplexer and current value register of state signals, CC are comparison circuits. The current values of state signals from the CVR outputs and the corresponding basic values from the RAM outputs arrive and are compared in the CC. In case of their anticoincidence the situation is analyzed by the processor. Further on the process is repeated.

The CDM is realized on 128 input channels.

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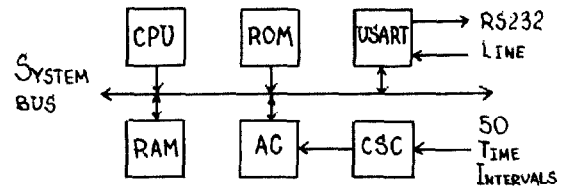


FIG. 1

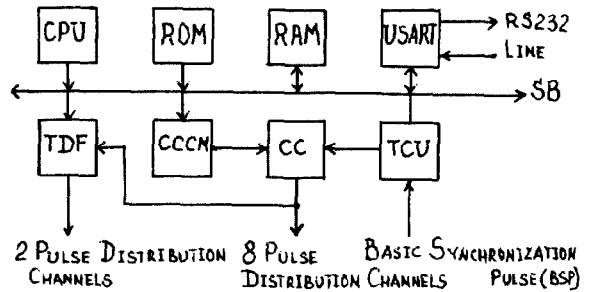


FIG. 2

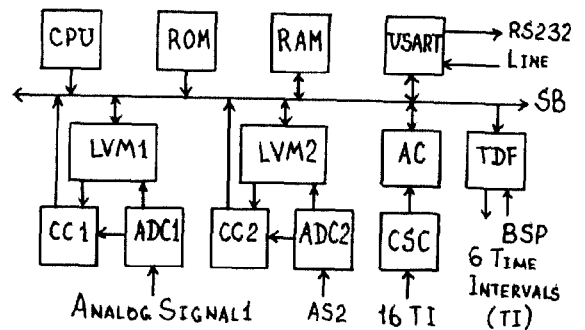


FIG. 3

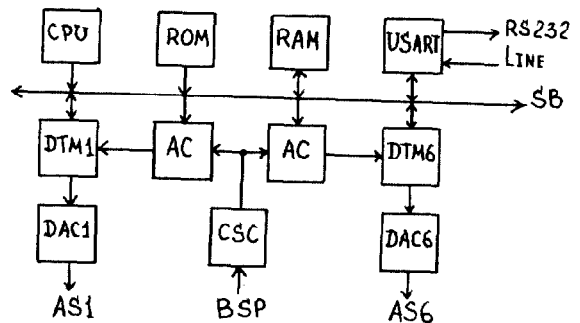


FIG. 4

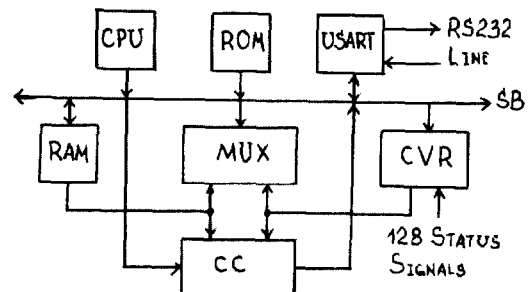


FIG. 5