Controls and Interlocks for a Prototype 1MHz Beam Chopper

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Abstract

A prototype 1MHz beam chopper for the proposed KAON Factory at TRIUMF has been constructed. The chopper is an electric field device, driven by a tetrode based pulser, for deflecting a charged particle beam. Associated with the tetrode used in the prototype design are high voltage power supplies for the electrodes. We use an FET based grid pulser and a sequencer capable of accurate digital control of pulse timing to 0.4ns. A safety interlock and control system using a programmable controlller with fibre optic links has been built. This has given us the versatility required in a prototype system.

I. INTRODUCTION

For ring-to-ring transfers in the KAON factory at TRIUMF Kicker magnets will be required. The TRIUMF cyclotron will be used as an injector for the synchrotron. To prevent beam spill at the transfer points, gaps must be introduced into the injected beam of sufficient duration to allow the kicker magnets to switch on and off. These gaps are produced using an electric kicker[1] operating at up to 15Kv. The repetition rate will be 1.022 MHz with alternate pulses of 46ns and 92ns. The field between the deflector plates must rise and fall in less than 39ns.

The electrical pulses that produce this field are stored in a low loss transmission line with a one-way propagation time of 1μs. One end of the transmission line is terminated with the deflector plates while the other is terminated with a short circuit. The line is centre fed by a tetrode whose cathode is at a high negative voltage. The complex reflections from the open and short circuited ends allow a single tetrode to function both as a charger and as a clipper depending upon the polarity of the reflected pulses. This device is described in a separate paper at this conference[2].

In order to operate the equipment safely, proper procedures as well as a safety interlock and control system were required. In anticipation of frequent changes to the prototype we chose to use a programmable controller (PLC) for the interlock system. PLCs are easily programmed using ladder diagrams and feature relay logic, timers and counters. Only a modest number of I/O points are required so the decision was taken to use an Allen Bradley SLC 150[3]. It has the advantage of low cost and small panel size and provides 20 optically isolated inputs and 12 isolated relay outputs.

The pulse sequences required to drive the tetrode were generated using reprogrammable PALs and programmable delays to produce pulses of arbitrary duty cycle and repetition rate (fig 1). The sequencer output was connected to a FET based grid pulser using fibre optics giving the required high voltage isolation and good noise immunity.

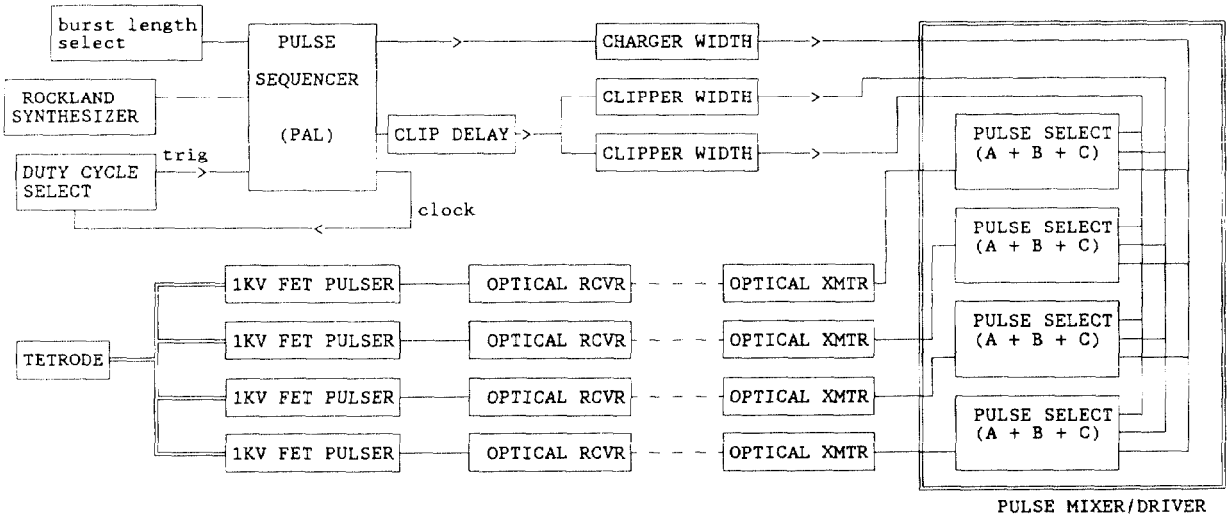

fig 1 Block Diagram of the Grid Pulse Sequencer

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II. GRID PULSER

The pulser is required to produce a pulse of magnitude up to 800v at the control grid with a rise time in the 10ns range. The quality of the pulse within the centre fed transmission line is extremely sensitive to the phase and frequency of the grid pulse. A variation of 3ns in timing typically added 10-15ns to the rise time of the stored pulse. It was therefore extremely important to maintain a stable pulse train capable of adjustments in sub-nanosecond increments. To realise this we used a Rockland frequency synthesizer as the rf source and digitally programmable delay lines for pulse timing. The high precision delay lines used (AD9501) are capable of delay increments as small as 10ps.

Sequencer

One operating mode requires a sequence of alternating charger pulses and clipper pulses. This is shown in the lattice diagram fig 2. We can launch a second chopper pulse at the null points when the inverted reflection from the short circuited end of the transmission line cancels the pulse reflected from the open circuit end. This effectively doubles the amplitude of the pulses in the transmission line. In this mode we require a pulse train of two charger pulses followed by two clipper pulses fig 3.

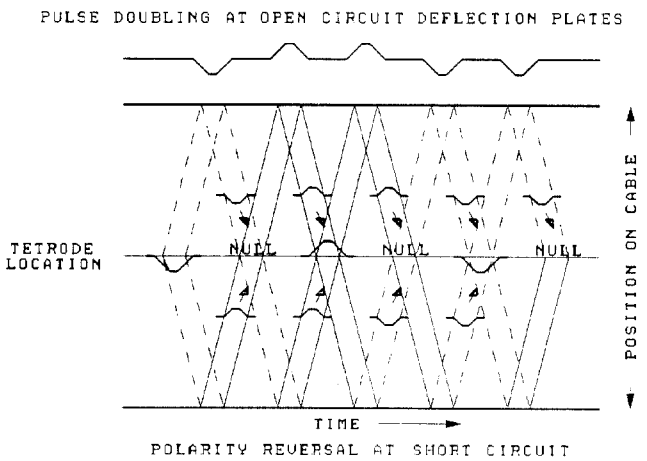


fig 2 Lattice Diagram

A programmable logic array device (PAL22V10) incorporating a counter and state machine controls the pulse mode and pulse burst length. An external counter determines the duty cycle by controlling the frequency of the burst trigger.

The timing and width of each pulse train may be independently adjusted before they are muliplexed and transmitted by a 100Mb optical fibre link to the FET pulser units. Fig 4 shows the transmitter pulse (top trace) and

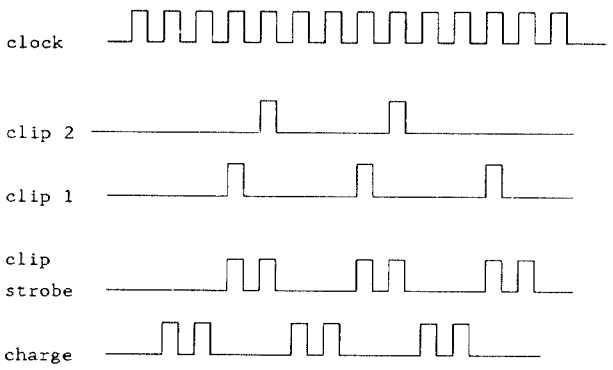
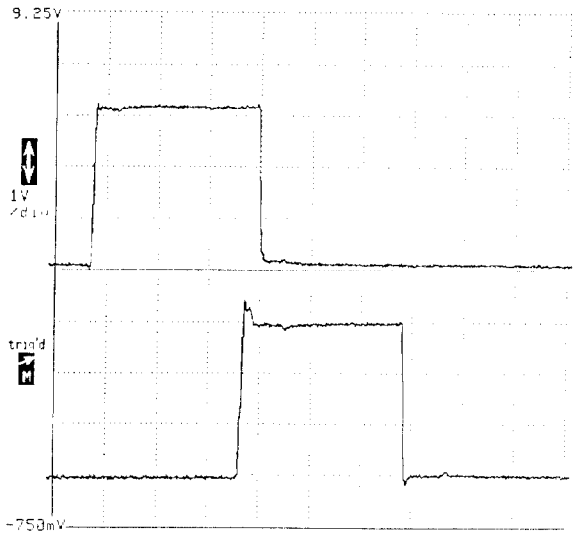


Fig 3 Sequencer output

optical receiver output pulse (bottom trace). We use DIP switches to independently select incremental delays and pulse widths with a precision of 0.4 nanoseconds.



Rise Time	Fall Time	Width
3.254 ns	1.941 ns	127.5 ns

Fig 4 Optical Transceiver Pulses

FET Pulser

This device is built around a DEI 150FPS mosfet driver[4]. This board is capable of driving high voltage FETs at frequencies up to 25MHz with pulse widths of 25ns and rise times of 3-5 ns. We use four pulser units connected in parallel with 50 ohm cable. Equation 1 shows that for a grid capacitance of 700pf we are limited to a rise time of about 10ns at the grid.

$$zc = \frac{50\Omega \times 700pf}{4} \qquad (1)$$

The four pulser units operate with a common but variable source voltage to a maximum of -800 volts. In addition the drain voltage of one of the units is variable while the remainder are fixed at ground. The pulser outputs are connected to a summing point close to the grid by coaxial cable. The pulse mixer and the four FET pulser units allows us to produce a composite grid pulse at the control grid of the tetrode.

III. INTERLOCKS

The Programmable Controller.

The traditional way to implement a safety interlock system is with relay logic, a time consuming and very inflexible method. For larger applications we have used a variety of embedded processors and a high level language. This approach while providing sufficient flexibility does not provide for rapid changes. For this reason we chose the SLC 150. As this compact unit already provided sufficient I/O capability for our purpose no further investment in hardware was required.

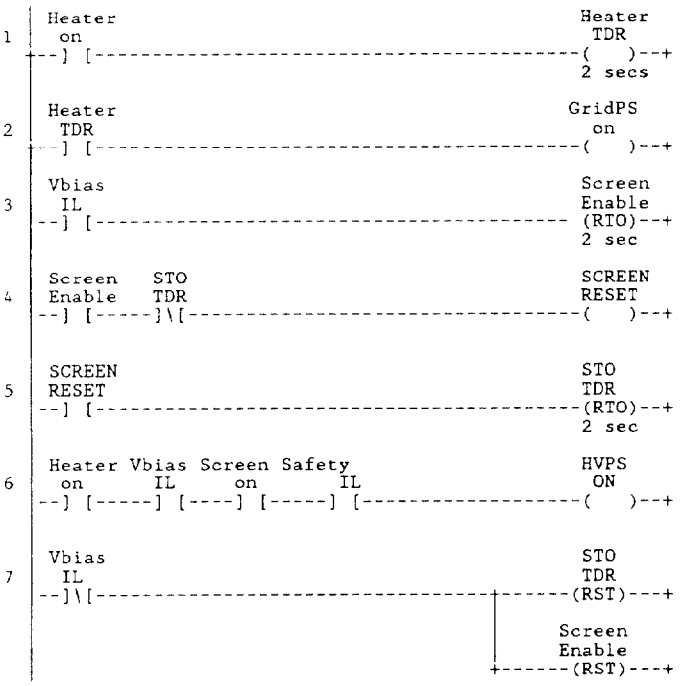


Fig 5 Power on sequence

Programming

The PLC was initially programmed using a PC-AT. The supplied software allowed off-line program development as well as downloading, on-line monitoring and storage. It was not always possible or desirable to permanently connect the PC to the system. For such circumstances a hand held keypad was used. This allowed rapid program changes to be made in the field. The PLC also had an interlock defeat feature and password protection.

The Program

The basic program insures that no high voltage power supplies may be energized until all cabinet doors are closed, the tetrode filament is on, the screen and control grids are biased and the cooling system functioning. Internal counters simulate time delay relays to control the startup and shutdown sequence. Fig 5 illustrates the use of these timers to control switch-on of the screen grid.

A time delay relay (TDR) insures a 10 minute warm up period for the tube heaters before the grid power supplies are energized (rungs 1 and 2). When the control grid bias voltage stabilizes a 2 second delay (rung 3) is initiated before a screen trip reset is generated (rung 4). This in turn starts a second TDR (rung 5) which gates off screen reset after 2 seconds (rung 4). At this stage the main high voltage power supply is enabled (rung 6). Loss of grid bias resets the TDRs ready for a new power up sequence. Should at any time a screen trip occur, the operator is forced to switch off the control grid and to go through the grid supply start up procedure in order to recover from the trip.

IV. CONCLUSIONS

Resources available to us during chopper prototype development were limited so we elected to use commercially available sub-systems wherever feasible. This approach has been vital in commissioning and testing the chopper. It allowed new functionality to be added with minimal disturbance. The components and techniques employed will be used in the design and development of a fully integrated chopper and kicker magnet control system at KAON.

V. REFERENCES

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