BPM DATA ACQUISITION SYSTEM FOR THE BATES PULSE STRETCHER RING

O. Calvo, T. Russ, J. Flanz
Massachusetts Institute of Technology
21 Manning Rd., Middleton, Ma. 01949

Abstract

A beam positioning monitoring system is being developed at Bates. It will include approximately 30 stripline monitors distributed around the South Hall Ring [3], These BPMs will be sampled by flash analog-to-digital converters operating at 40 MSPS. Each ADC is connected to a FIFO that can be read by the CPU (SparcStation in a single VME slot, running SunOS) and transferred via Ethernet to the central control system, after some local processing. Hardware and software operation of the prototype are described

I. Introduction

MITs Bates Accelerator Center is being upgraded to provide high duty factor CW electron and photon beams of excellent quality, with energies up to 1 GeV, for use in nuclear physics. This pulse strecher ring will extend the beam duty factor to 85 %, with a maximum extracted current of 50 uA. It will also initiate a program of internal target studies when operating in storage mode. Operation is based on repetitive injection (up to 1000 times a second) of a short high peak current pulse (40 mA) during two turns, followed by time-uniform extraction of the stored beam during the interpulse period.

Beam position monitors will be used in different stages of the operation of the machine. In the initial turn-on, they will be used to steer the beam clear of all apertures during injection, and to find the closed orbit, measure the integer and fractional part of the tune, obtain the beta functions and identify instabilities during storage and tune-up. During extraction, they will facilitate the measurements of dynamic aperture, the adjustment of the non-linear elements and the fractional tune, and the optimization of the extracted beam with fast-feedback and feed forward loops. In normal operation, the BPMs are mainly used to determine beam position, phase space and fractional part of the tune.

II. Beam pick-ups

There are thirty one BPMs in the ring (roughly four per betatron wavelength). They have a resolution of +/- 0.1 mm with circulating currents ranging from 1 to 80 mA. We are currently testing a prototype detector made of two pairs of 50 ohms, 3/4 lambda striplines with a position sensitivity of 400 mV/mm. The signals from all detectors are processed by amplitude-to-phase modulation (AM/PM) modules, downconverting the RF signals to 50 MHz with an analog bandwidth around 20 MHz. These detectors also provide a current output delivering 40 mV per mA of beam current. A button detector is also under development. It has lower output signal levels but is far less disturbing to the beam and could be easier to manufacture[2].

III. Analog to digital Conversion

Each BPM has three channels: two corresponding to vertical and horizontal positions and a third one indicating the beam current. (Fig. 1).

Analog signals coming from the detectors are amplified, offset and sampled by flash analog-to-digital converters, operating at 40 MHz. After testing four different units we settled for the Analog Devices AD9012, which offers a maximum frequency of 75 MHz and is TTL compatible. Each ADC is connected to a high speed FIFO that can be read by the local processor. Information on the FIFOs is read into main memory by a real -time processor residing in the VMEbus. This data is locally processed and the results are sent to the central control system. By using PLCC packages we can integrate nine channels in a 6U, B size VME card. The goal is to put as many as 150 channels in a single VME crate.

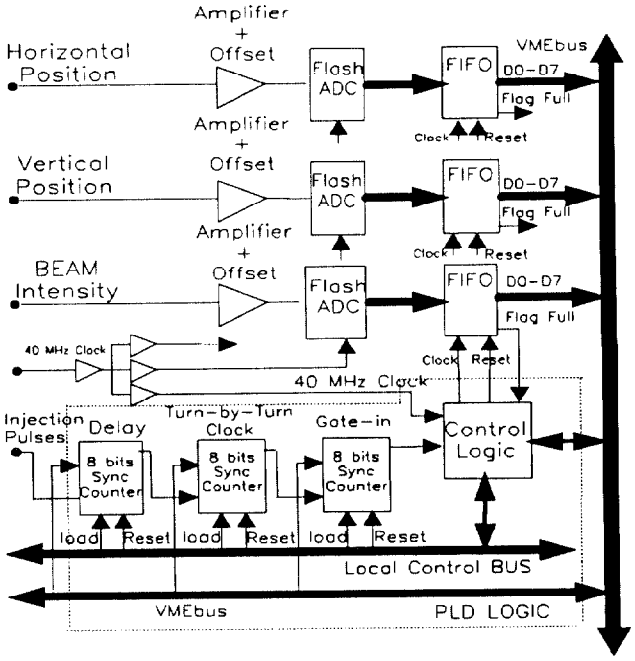

Figure 1. ADC channels and triggering logic

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IV. Triggering Logic

The A/D converters are free running at maximum speed, and it is the responsibility of the triggering logic to decide when to latch the data on the FIFOS. Any BPM can be programmed independently of the others to operate in different modes. The main trigger pulse that activates all the channels is also synchronized to and delayed from the injection pulse. A separate timing card is in charge of this function and distributes the timing pulses to all the channels. This board has interrupt generation capabilities, and also provides the timing to the VME processor unit. The main 40 MHz clock is derived from the main RF frequency (2856 MHz) through a PLL divider/multiplier.

Different lengths between cables, and beam delay, can produce time mismatches between channels as large as 800 ns (more than one turn). These delays are compensated in two steps. First, the cables are trimmed so that the delay between channels is always an integer multiple of 25 ns. Then, 6 bit programmable digital delays are set from the control system to any number of 25 ns. intervals between zero and 64 (zero to 1.6 usec) (figure 2). The turn by turn (TBT) clock is obtained by dividing the 40 MHz sample signal by 25. Each bpm has its own set of counters implemented with high speed PLDs (Xilinix 3020). This solution presents more flexibility than using conventional logic: changes in trigger circuitry can be done by merely reprogramming the PLDs.

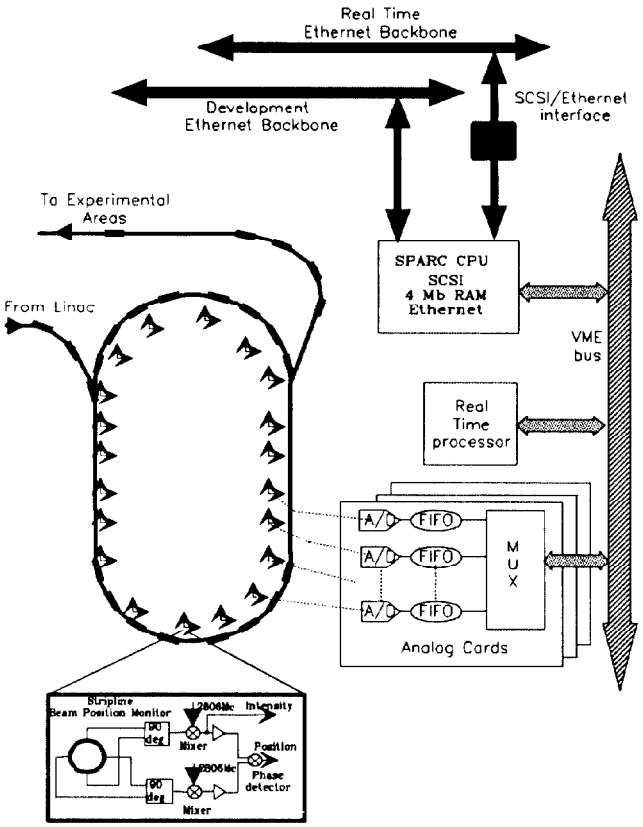

Figure 2. Overall Layout

By avoiding LC delay lines and making all data capturing synchronous, the design of the timing generation functions is greatly simplified.

V. Data Processing

The main processor is based on the SPARC 1E, VME based CPU. This microcomputer engine can run SunOS (Unix). It operates at 20 MHz, delivering 12.5 MIPS with a floating point capacity of 1.33 MFLOPS, and has 4 Mbytes of RAM, a SCSI and an Ethernet port. It can be easily linked to our instrumentation computer, a SUN SparcStation two [3].

Since both computers, target and workstation are basically identical, all the software development can be done either in the workstation and then ported to the target, or in the target itself, across the network. During the software development stage, a private Ethernet connection will be used to link both systems. If future application require it, this "private network" can be used for "heavy" data logging without saturating the main control system Ethernet network.

Having the Workstation "right on the bus", controlling the instruments directly, significantly increases the power of analysis. Otherwise, only relevant data would be available to the instrumentation computer and most of the raw data would be thrown away.

VI. Software

All the software is being written in ``C'' and runs under SunOS. Benchmarks run on the SparcEngine indicate that a hardware interrupt, requested from the VMEbus, can be serviced in 16 usec . A very small routine decodes the command issued in the main console of the control system, encoded in a low level Ethernet packet. A SCSI to Ethernet adapter, developed in house,allows us to transfer data to the network only during a certain time window, minimizing collisions and improving the effective bandwidth.

The software is also responsible for setting the channels to its proper mode of operation., loading all the delays, arming the trigger, transferring the data from the FIFOs to main memory, averaging out the data and performing mathematical computations, such as FFTs.

VII. BPM Measurement Modes

As stated above, the bpms will operate in very different modes depending on the status of the machine:

A. Integer Tune - All BPMs at one time

The purpose of this measurement mode is to obtain a snapshot of the trajectory of the beam during one complete turn. Thirty one BPMs (93 channels), distributed around the ring are sampled at the same time, allowing us to determine

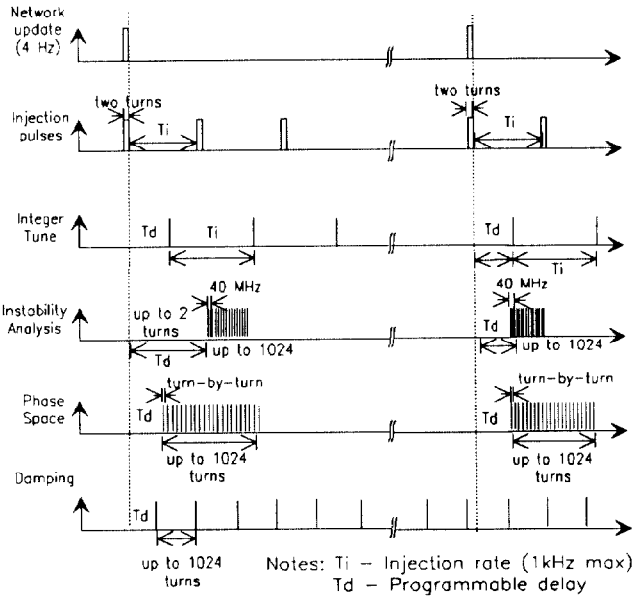

Figure 3. BPM timing diagram

the betatron oscillations. The sampling process is triggered by the injection pulse and delayed a number of turns specified by the operator (up to 1800 turns for 1 KHz injection rate). This is applicable to all the measurement modes. The previous process can be repeated at injection rate for data averaging. Only averaged data will be sent to the network.

B. *Instability analysis and fractional part of the tune.- One BPM vs time*

In this mode of operation, selected BPMs are sampled at 40 MSPS until the FIFOs are full. An FFT will be calculated on these points. The sampling frequency was chosen to measure frequency components as high as seven times the revolution frequency (1.58 MHz). To be conservative, the sampling frequency is 40 MHz, providing an theoretical analog bandwidth of 20 MHz. This means that there will be 25 samples per turn.

C. *Phase Space - Two BPMs, turn by turn.*

In this mode, position and angle are of interest. Two BPMs are monitored, once every turn (turn rate) until the FIFOS are full (1024 turns). The results of this measurement are updated at 4 Hz rate until a new mode is selected.

D. *Damping - One BPM, turn by turn.*

This mode is similar to the phase space measurement, except that only one monitor is necessary and the samples are stored in main memory every N turns, where N is user selectable. Injection rate is very slow and the number of samples stored is also user selectable.

E. *BPMs in the Injection line*

Five BPMs are located in the injection line. They work with a pulsed beam and operate in two different modes.

1. *Normal operation - Injection rate*

Under normal operations, these BPMs are sampled at a rate of one per injection pulse. The sampling point must fall in the middle of the injection pulse.

2. *Fast Plot mode*

In this mode, all the BPMs are sampled at maximum speed during two turns. This is done only once, and the data is sent to the network for plotting. No averaging is necessary. FIFOs will be refreshed at their maximum allowable speed rate.

VIII. Conclusion

The system described is currently under development and will be operational in 1992. A prototype of the flash ADC was built and will be tested soon with the pick-ups located in the Bates Linac. A video matrix switch was also developed to allow the selection of 16 out of 256 signals to be brought to the control room, simplifying the analog monitoring of bpm signals.

The Unix machine on the VME bus reduces enormously the development time and the use of a standard operating system facilitates the communication with the host

The combination of a flash ADC, FIFO and flexible trigger multiplies the capabilities of the acquisition modes. Once the ring enters in operation, new measurement modes could be requested, which can be easily inplemented through reprogramming of the PLD logic.

IX. References

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