A 256 Channel Digital Filter for a Data Acquisition System

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Abstract

The TRIUMF Central Control System (CCS) employs several data acquisition systems to monitor its operational parameters. Each system multiplexes 256 analog channels into one analog to digital converter. Space constraints on the multiplexer cards prohibit the installation of adequate anti-alias filters which allows 60 Hz and other noise to corrupt the measurements. The new system overcomes this problem by sampling each channel at a 160 samples/second rate and using a DSP microcomputer to lowpass filter the data. The multiplexer and analog-digital converter operate at 256 times the channel sample rate. The channel filter bandwidth is restricted to approximately 1 Hz due to the rate at which the CCS reads the data. One DSP microcomputer is able to filter the 256 channels in a multiplexed system at a cost less than that of the anti-alias filters which would otherwise have been required.

I. INTRODUCTION

The TRIUMF Cyclotron requires many channels of low speed data acquisition for control and supervisory purposes. The CCS acquires these signals though systems of multiplexed analog-digital converters (ADC). The multiplexer preceding the ADC has 2 stages of 16 to 1 multiplexing for a total of 256 differential channels. In this system the desired signals are essentially dc but are accompanied by noise with a much greater bandwidth. Since this is a sampled data system the possibility of the noise being aliased into the signal bandwidth must be considered.

Sampled data systems acquire data at discrete time intervals of $1/f_s$ where f_s is the sampling frequency. Sampling is equivalent to modulating an impulse function by the input signal. The input signal is replicated around the multiples of the impulse frequency [1]. All signal and noise components at the input to the sampler are translated into the frequency band 0 to $f_s/2$ (the Nyquist frequency) unless filtered out before they are sampled. If the input signal bandwidth is greater than $f_s/2$ the signal components greater than $f_s/2$ are added to those between 0 and $f_s/2$. Figure 1 shows the effect of sampling the signal $1 + 0.1 \sin(2\pi 60t_s)$ at a sampling frequency of 3 samples per second (SPS) with a uniformly distributed jitter of 1% of the sample frequency. The result is a noisy looking signal with an mean value of 1. The noise which was originally a 60 Hz sinewave is now a random signal which may be difficult to filter out to the required degree. The worst case occurs when the sampling frequency is an exact submultiple of the signal frequency. In this situation each sample is at the same point on the waveform and thus leads to a dc offset at the sampler or ADC output.

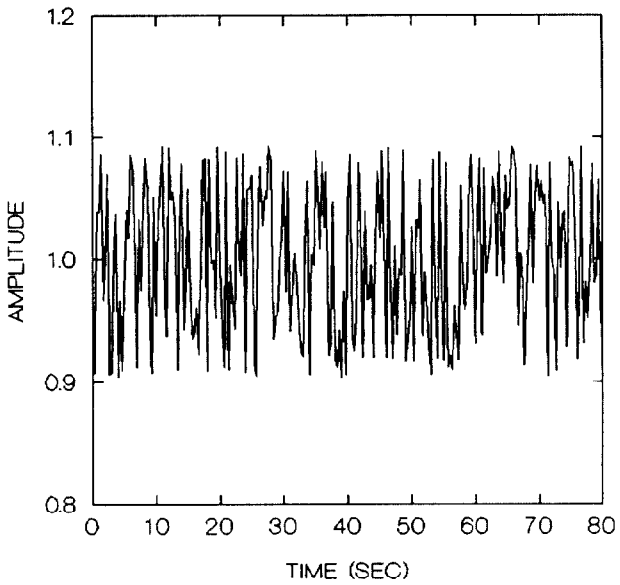

Figure 1. Sampling 60 Hz at 3 +/- .03 SPS

This demonstrates the need to prevent aliasing. Noise which may be easily separated from the signal before sampling may be difficult or impossible to filter out after sampling. In the present CCS multiplexer system the input filtering on each channel consists of a single pole RC lowpass filter with a cutoff frequency of 3.6 Hz. Although the multiplexer system is differential up to the ADC it is inevitable that 60 Hz and other noise will enter the system at different points. The upgrade to the present system replaces the 12 bit ADC with a 14 bit device for increased resolution of low level signals. A 14 bit ADC has a dynamic range of ± 78 dB, therefore, even a small 60 Hz component at the input can mask a large part of the ADC dynamic range. The RC input filters attenuate 60 Hz components by a factor of 0.06 before sampling and digitizing occur but this is not good enough in a high resolution system sampled at 3 SPS.

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An anti-aliasing filter is required to prevent this translation of the noise frequencies into the measurement frequency range. It is not possible to construct adequate filters for each channel on the multiplexer cards due to space and cost constraints. The alternative described here implements the anti-aliasing filter after the ADC conversion. In this configuration the ADC is required to sample at a rate much higher than the final sample rate of 3 SPS and then filter the sampled signal to a bandwidth of about 1 Hz. This meets the anti-aliasing requirements for the CCS sampling rate. The front-end RC filter protects the ADC from aliasing since its cutoff frequency is much less than the ADC sampling frequency. The advantage of this method over a purely analog method is that one digital filter can be shared among the 256 multiplexer channels at a significant saving in space and cost.

II. DIGITAL FILTER

The digital filter is implemented in a single Analog Devices ADSP-2105 DSP microcomputer [2]. This device has sufficient internal program memory to contain the filter algorithms. External data memory contains the ADC data and intermediate results. An external dual-port memory is used to transfer the final results to the CCS. The filtering is done in 2 stages in order to reduce data memory requirements and the computational load. The first stage sample frequency is much higher than the final system bandwidth. This is to allow the input RC filter to provide adequate anti-alias filtering for the ADC. This high sample frequency, however, requires many coefficients to reduce the bandwidth to the required value. A low cutoff frequency is more easily attained by sampling at a lower frequency but this cannot be done by simply throwing away unwanted samples since is the same as sampling at a lower rate and aliasing will occur. This 2 stage approach uses finite impulse response (FIR) filters of 22 and 26 coefficients whereas the equivalent single stage FIR filter would use more than 128 coefficients.

The function of the first stage filter is to provide anti-alias filtering for the second stage which can then sample the output of the first stage at a lower sampling rate. This lowpass filtering and resampling at a lower rate is referred to as decimation [3]. A reduction in the decimation stage computational load is attained because the output of the stage only needs to be computed at the second stage sampling rate not at the first stage sampling rate. The function of the second stage is to limit the system bandwidth to a value consistent with the CCS sampling rate.

The first stage filter is equivalent to 3 cascaded n point moving average filters where n = 8. The desirable characteristic of this filter are the notches at intervals of f_s/n in the frequency domain. In this case the sampling rate is 160 SPS giving notches at multiples of 20 Hz. Figure 2 shows the frequency responses of the 2 filter stages. One function of the notches is to eliminate 60 Hz and its harmonics on the assumption that these are main discrete noise sources. 120 Hz and 180 Hz are greater than the Nyquist frequency but they are aliased to 40 Hz and 20 Hz respectively where notches exist. The other function of the multiple notch response is to provide anti-alias filtering for the second stage. This is shown in Figure 2 where the first stage notches coincide with the second stage passbands and eliminate any noise that would be translated into the second stage passband. The only unprotected regions are around multiples of the first stage sampling frequency which coincide with passbands of the second stage but these are narrow regions and are attenuated at higher frequencies by the input RC filter.

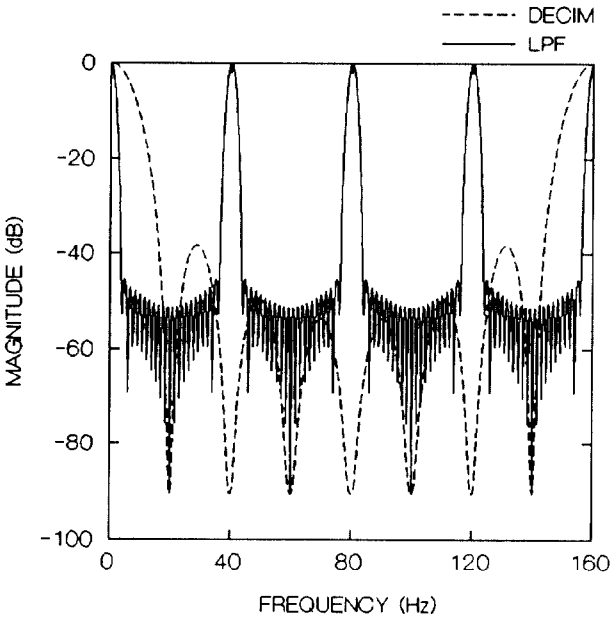

Figure 2. DECIMation, LowPass Filter responses

The second stage is a lowpass filter with a cutoff frequency of 1 Hz. The sampling rate is 40 SPS or 1/4 of the first stage sampling rate. The primary reason for reducing the sample rate is that a 1 Hz cutoff can be achieved more efficiently, in terms of the number of filter coefficients, than would be possible with a 160 SPS sampling rate. A secondary reason is the gain in computing efficiency since only every fourth output from the first stage needs to be calculated. The remaining three output values are not used although all the input data samples are needed to calculate the output values. The lower limit on the sample rate of this stage is the requirement to update the output data as fast as the CCS samples it. A conflicting constraint

is to reduce the time delay of the filter, which is product of half the filter length and the sample interval, to a value which will not be noticed by the machine operators. This requires a higher sample rate for the same length filter. For the filter length and sample rate chosen in this case the delay through the filter is equivalent to 2 CCS sample periods.

A characteristic of digital filters is that the frequency response repeats around multiples of the sampling frequency as is seen in Figure 2 where the second stage response is shown out to 4 times the second stage sampling frequency. This shows the need for the preceding anti-aliasing stage.

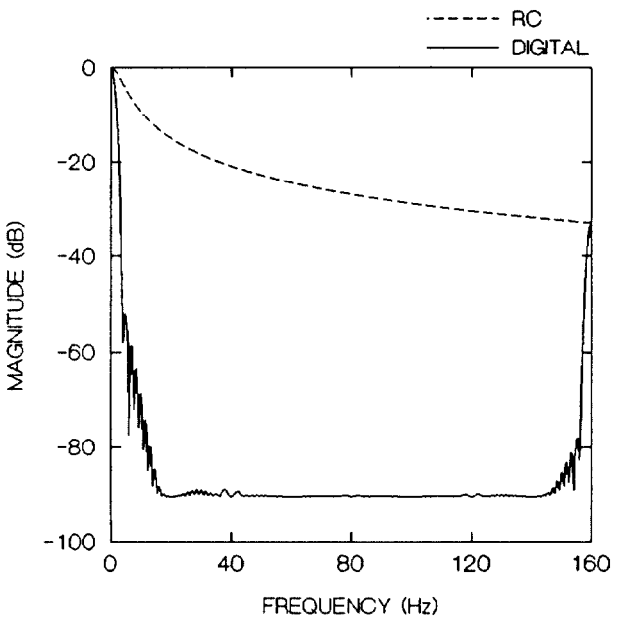

Figure 3. Digital, RC filter responses

The system bandwidth has now been reduced by the second stage to 1 Hz which meets the anti-aliasing requirements for the CCS data acquisition system. Figure 3 shows the combined response for the RC and digital filters compared with the RC filter response alone. There is an improvement of 19.5 dB in noise rejection over the 0 to 160 Hz range. The anti-aliasing effect of the RC filter is seen in the attenuation of the passband at 160 Hz where the envelope of the digital filter response follows the RC filter response. The stopband floor of -90 dB is due to noise added to the plot to simulate the limits of the 16 bit arithmetic results of the DSP processor. Intermediate results in each filter stage are calculated to 32 bits before rounding to the 16 bit result. Higher precision arithmetic would lower the noise floor but to no advantage since the CCS is a 16 bit system.

III. Design and Test

The filters were designed and evaluated using the Signal Processing Toolbox for PC-MATLAB [4]. This allowed comparisons of different filter orders and architectures. A prototype system consisting of ADSP-2101 and Crystal Semiconductor CS5016 ADC evaluation boards verified the frequency response and multichannel operation of the filter system at full speed. Less than 25% of the available DSP processor cycles are needed for this system.

IV. Summary

Sampled data systems are subject to a form of signal corruption termed aliasing. The bandwidths of the system and of the anti-alias filter are related to the use of the resulting signal. An operator looking at the data at a rate of once every few minutes is also sampling it. In this situation the bandwidth should theoretically be restricted to a fraction of a Hertz. The same operator watching the data while adjusting a machine parameter wants a wider bandwidth to follow the results of the adjustments more closely. The choice of sampling rate and bandwidth must be based on the bandwidths of the signal and noise, the required time response of the data acquisition system and the uses of the information. In this case the CCS sampling rate and dc nature of the signals determined the system bandwidth. Space constraints on the anti-aliasing filters in the multichannel system led to the design of a digital anti-alias filter based on initial oversampling and subsequent decimation and lowpass filtering.

V. References

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