INDIRECT PHASE LOCKING OF RF CLOCK TO THE BEAM FOR BNL BOOSTER BPM SYSTEM.*

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INTRODUCTION

The beam position monitoring (BPM) system for the BNL Booster consists of 48 main pick-up electrodes (PUE) symmetrically distributed around the ring and two special PUE's for the transverse dampers. The BPM system utilizes an integrator that is AC coupled to the PUE. In order to eliminate the cumulative error in the signal from the PUE introduced by the AC coupling, a base line restorer (BLR) is used to reestablish a reference value between the bunches. Three signals phase locked to the beam, 48 x f_{REV} and both quadrature components of f_{RF}, are needed to insure that the triggers to the BLR's occur between bunches. The triggers for the main PUE's require a clock at 48 times the revolution frequency as well as the RF frequency to time their occurrence. The quadrature components of RF frequency are used in a phase shifter to produce the triggers for the damper PUE's. By making use of direct digital synthesis technology, we were able to produce all three signals locked to the beam using only a single phase locked loop.

DDS OPERATION

The operation of our design relies upon the use of direct digital synthesis. A direct digital synthesizer (DDS) reproduces a sinusoid of a specific frequency from the digitally generated samples of that signal. As shown in the block diagram (Fig. 1) the heart of a DDS is a numerically controlled oscillator (NCO).The digital data loaded into the delta-phase register is the phase step that will be added to the phase accumulator on each clock pulse. The phase accumulator is used to address a look-up table which contains the amplitude of a sinusoid as a function of phase, accomplishing a phase to amplitude conversion. This digital value is then passed through a DAC to produce an analog signal. According to the sampling theorem, a sinusoid of the desired frequency can be extracted from this signal by filtering out all higher harmonics provided the sampling rate is greater than twice the frequency of the sinusoid. This translates to a maximum frequency output of half the clock frequency. Thus, the output frequency, f_o, depends on how often the phase accumulator is updated (f_{CLOCK}) and the size of each phase step (eq. 1).

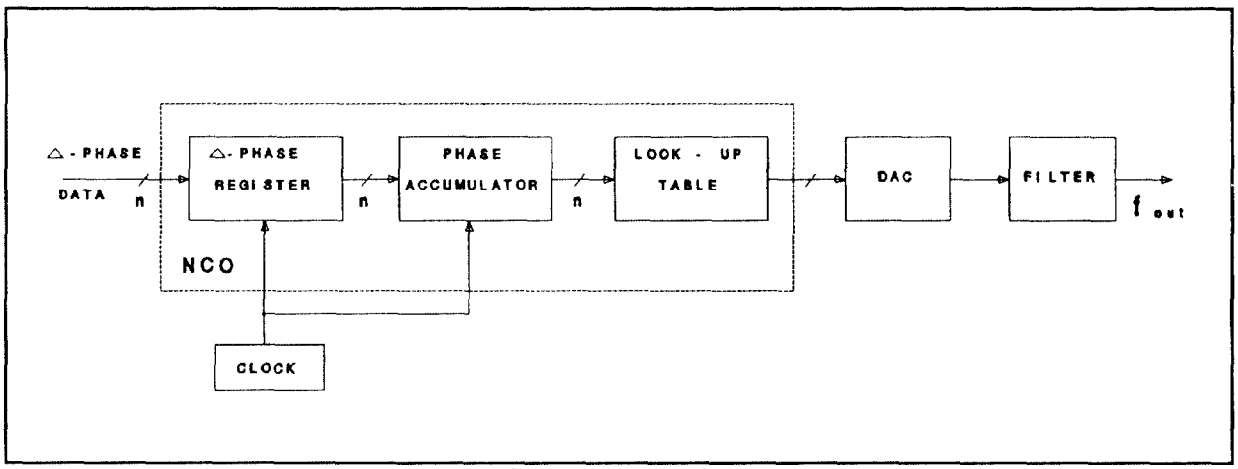

Figure 1. DDS Block Diagram

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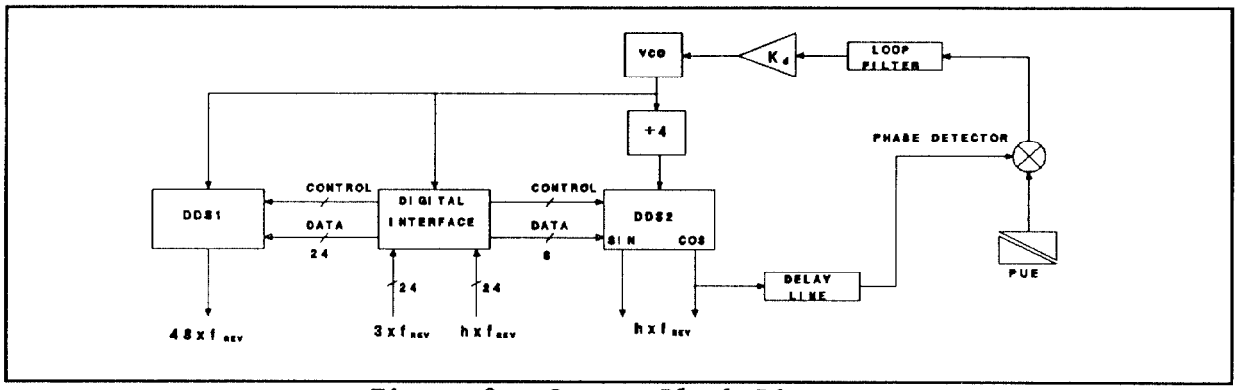

Figure 2. System Block Diagram

$$f_o = \frac{f_{CLOCK} \times \text{delta-phase}}{2^n} \quad (1)$$

Quadrature outputs can be obtained by using the phase accumulator to address two look-up tables, one with sinusoidal amplitude information and the other with cosinusoidal amplitude information. Each signal is then separately passed through a DAC and filtered.

SYSTEM DESCRIPTION

As shown on the block diagram of the system (Fig. 2) the VCO is used directly as the 200 MHz clock for DDS1 and is divided by four to provide the 50 MHz clock for DDS2. Therefore, for the same digital word (i.e. delta-phase step), the output frequency of the first synthesizer will be four times that of the second synthesizer. Also, as long as the digital words are exact multiples, the two outputs will remain phase locked.

The data for the two DDS's is received by the digital interface as two 24 bit words from an external frequency look-up table. The received data word for DDS1 is always 3 x f_{REV}. The received data word for DDS2 is h x f_{REV} (i.e. f_{RF}), where the harmonic number, h, is 3 when the machine is accelerating protons and switches from 12 to 3 during the acceleration of heavy ions. Thus, the two incoming digital words are identical for h = 3 and differ by exactly a factor of four for h = 12. A two bit shift to the left is introduced in the digital interface before the data is loaded into DDS1, so that the data now corresponds to 12 x f_{REV}. However, this frequency is based on the 50 MHz clock that DDS2 is running on. Since the clock for DDS1 is running at 200 MHz, the actual output frequency is the desired 48 x f_{REV}. Clearly, since the digital words are exact multiples and a common clock is used, the output of DDS1 and the quadrature outputs of DDS2 are phase locked regardless of variations in the VCO frequency.

In order to lock these signals to the beam, a phase locked loop is closed between one of the quadrature outputs of f_{RF} from DDS2 and the beam signal from a PUE. To simplify the design of the loop and to facilitate filtering the beam harmonics from the PUE signal, both signals are mixed up to an intermediate frequency of 10.7 MHz. Another design consideration for the loop was the need for a 1.5 μs delay line to compensate for the distance between the PUE and the DDS chassis, which effected the stability of the loop. In order to reduce the phase error accumulated over the RF frequency sweep, an active filter was chosen for the loop filter.

A unique feature of the phase loop is that the tracking range is not a constant but rather is a function of the frequency. In a standard phase locked loop:

$$\Delta f = k_d V_c$$

where k_d = gain of the VCO
V_c = VCO control voltage

However, in this loop, varying the VCO control voltage has the following effect on frequency:

$$\Delta f = \left(\frac{\text{delta-phase} \times f_{CLOCK}}{2^n}\right) \times V_c$$

Thus, the tracking range and the gain of the loop are directly proportional to the output frequency.

RESULTS

In order to test our system prior to Booster commissioning, we used an external source to simulate the beam signal. By introducing a frequency error into the external source, we were able to test the operation of our system. While sweeping over the Booster proton cycle from 2.4 - 4.2 MHz, a frequency error was introduced (Fig. 3). There was a maximum phase variation of less than 6° between sin f_{RF} and the "beam" signal (Fig. 4).

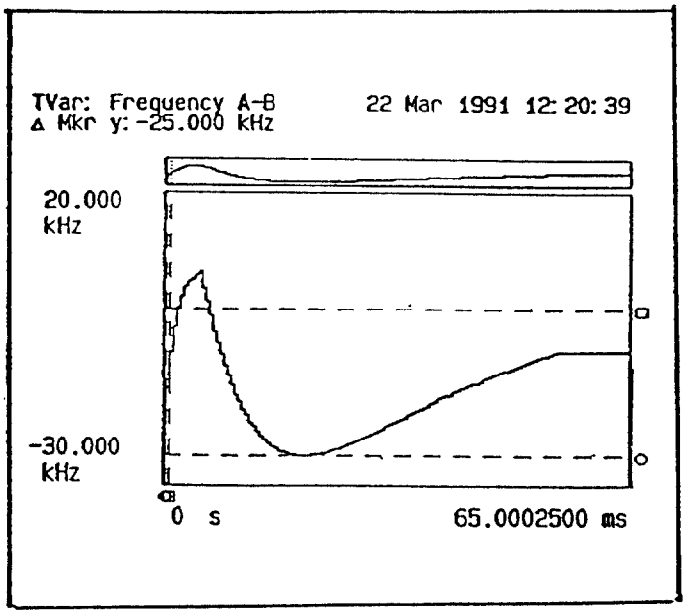

Figure 3. Open Loop Frequency Error

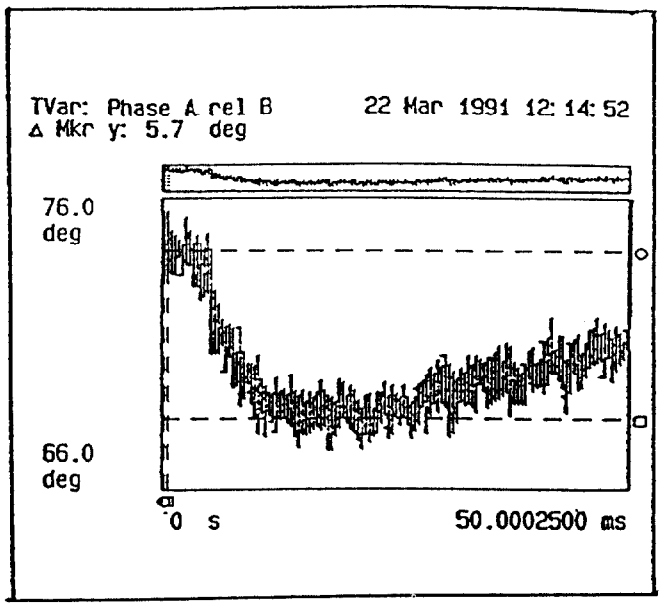

Figure 4. Phase of sin f_{RF} vs "beam"

CONCLUSION

By making use of DDS technology we successfully phase locked all 3 signals to the "beam", eliminating the need for three separate phase locked loops. Also, the use of direct digital synthesis provides quadrature outputs that are exactly 90° out of phase over the entire frequency range of the synthesizer. The only limitation of using this indirect phase-locking technique is the availability of high frequency DDS's.

ACKNOWLEDGEMENTS

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