

TUNE TRACKERS FOR THE FERMILAB TEVATRON

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Abstract

A system for continuous real time measurement of betatron tune has been developed and installed for the Fermilab Tevatron and Accumulator ring. A phase-locked loop, using a considerable amount of input signal preconditioning, is used to lock to a betatron oscillation harmonic in the Schottky detector output signal. This system has demonstrated the capability of measuring the Tevatron fractional tune to an accuracy of $\pm .002$ at 100 Hz bandwidth. The desired tune spectrum line has a very low signal to noise ratio, undesired revolution frequency harmonics, frequency modulation with wide deviations, and amplitude modulation with levels to 100%. Shown are the techniques used to overcome some of these limitations, with examples of the systems accuracy and tracking performance.

Introduction

The tune number is described as the number of betatron oscillations around one revolution of the ring, which is normally in the range of 19.35 to 19.45 for the Tevatron. It is commonly referred to by the fractional part of the number, symbolized by ν . The signal originates from a Schottky detector as a 21 MHz signal, a harmonic of the Tevatron 47 KHz revolution frequency (F_{rev}). This signal is down-converted in two stages by mixing with multiples of F_{rev} leaving a difference frequency of $\nu(F_{rev})$ or nominally 19 KHz.⁵ Measuring the frequency and scaling by a fixed value for F_{rev} produces the desired fractional tune value. This method allows the use of a low frequency spectrum analyzer to monitor the tune, however they are too slow for making fast time plots or for use in a possible feedback scheme. Another method is to use a phase-locked loop "tune tracker". Described in this report are the efforts to overcome some application problems and optimize the performance of a phase-locked loop (PLL) system.

Design Considerations

The Tevatron Signal:

1. The tune range of .35 to .45 for the Tevatron gives a tune signal range of 16.7 to 21.5 KHz.
2. The output amplitude level is nominally -20dBm, but ranges from -50 to 0 dBm depending on acceleration mode.

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3. The signal is normally only 3 to 10 dB above the noise floor. The S/N ratio is calculated from the ratio of the power spectrums² and typically has a value less than one.
4. Revolution frequency and betatron oscillation harmonics and sidebands are present at every $N(F_{rev})$. The largest of these is the tune signal image frequency at $(1-\nu)F_{rev}$ (26-31 KHz), (Fig. 1) and is about equal to the desired signal.
5. The signal is frequency modulated (FM), with a gaussian distribution of frequency components of 0 to 1KHz.
6. The signal is also amplitude modulated (AM), (Fig. 2) with levels reaching 100%, and with frequency components to 1KHz BW.

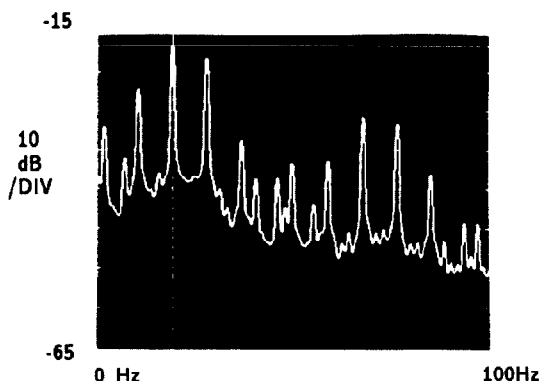


Fig. 1. Frequency spectrum of the tune signal, showing revolution frequency harmonics and sidebands present.

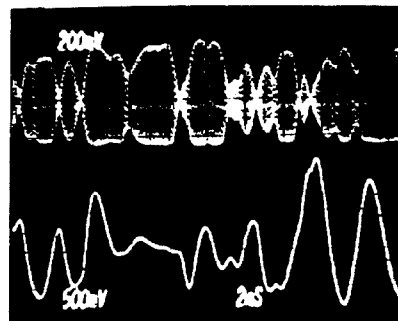


Fig. 2. Typical signal with 100% A.M. (top) and error signal of PLL trying to maintain lock to same signal.

For the Anti-Proton (AP) Accumulator ring a low frequency Schottky detector is used, with output at 245 KHz. A variation of the same PLL system is used, in this case without frequency conversion, but requiring a real time F_{rev} measurement. The AP signal is similar to the Tevatron signal except that it has a better signal to noise ratio and the undesirable harmonics are farther away.

Performance Goals:

1. Use a PLL circuit to measure the fractional tune of the Tevatron in real time with resolution and accuracy to within .002 fractional tune.
2. The dynamic response characteristics of PLL, must enable tracking a tune signal containing FM of 500 Hz bandwidth (BW), at a 100 Hz Mod. rate, maintaining accuracy, and FM of 6 KHz BW maintaining lock.
3. The PLL must lock to and track the tune signal from an initial unlock condition, at turn on, or for any frequency step within the tune range.
4. Provide a noise free output to indicate a "locked" condition.

Circuit Design

A review of PLL design theory shows the relative merits of the various types of circuits. There are many types of phase-detectors, but all can be classified as either linear or digital. The PLL textbooks^{1,2} strongly emphasize the use of a linear phase-detector for tracking filters, or for any application where the signal is buried in noise.

The digital detector, as its name implies, uses logic gates which are switched at threshold levels, zero crossings, or rising/falling edges. It is highly susceptible to any noise or jitter on the input signal at the threshold levels of the input comparator, while its internal logic functionally stores the resulting false triggers. The output uses logic levels with a varying duty cycle to indicate the phase error, again introducing uncorrelated digital noise.

The linear phase-detector is an analog device, usually a mixer or an integrated circuit multiplier, which actually multiplies the inputs together, giving an output product containing the phase error. Noise on the input signals has an effect on the output only in "linear" proportion to the relative noise power. Small glitches produce a corresponding small amount of phase noise, more readily reduced by the loop filter.

Several different types of phase-detectors were tried on the actual tune signals to check their performance. The above comments were verified, with the digital types able to maintain lock only about 75% of the time, compared to nearly 100% for the linear types. The linear detector however, is amplitude sensitive and since the input has a high level of AM and wide signal strength variation, additional conditioning circuitry is required. References^{3,5} indicated that the best performance would be obtained by using a limiter, rather than an automatic gain control circuit.

Shown in Fig. 3 is a block diagram of the Tevatron circuit. The overall circuit includes a narrow bandpass filter, a high gain limiter, and a linear phase-detector. The BPF, an 8th order Chebyshev, attenuates most undesirable harmonics by 40 to 70 dB. The preamp, filter and the limiter combine to produce a dynamic range of about 80 dB, with the PLL section maintaining lock.

The PLL circuit (Fig. 4) used in this system is a second-order type using an active loop filter. The circuit is constructed using separate IC's for the major components, to allow flexibility in the loop filter, loop gain and the output scaling. The loop filter natural frequency is set as low as possible (about 2 KHz), consistent with a damping factor of .7 and gain that allows sufficient tracking and lock in range. The PLL error voltage passes through final filters (post PLL BW limiting), and buffers to provide the outputs.

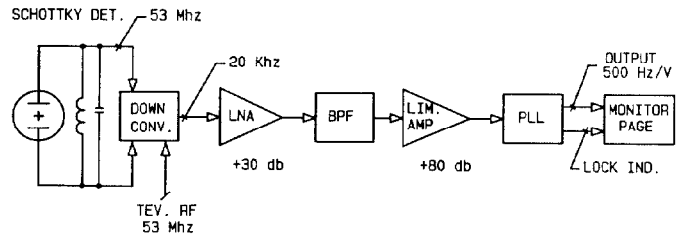


Fig.3. Block diagram of the Tevatron tune measurement system.

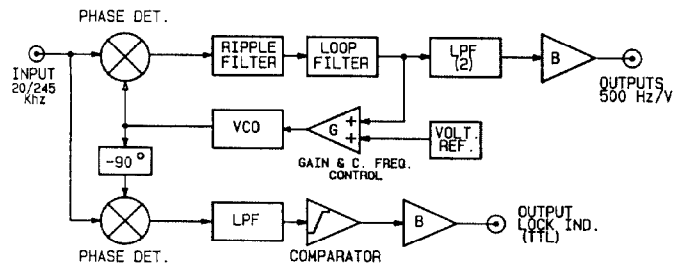


Fig.4. Block diagram of the phase-locked loop circuit.

Results

The performance was monitored during Collider operation and during a recent fixed target run where the "Tune" ranged from .45 at injection to .5 at extraction. Shown in Figs. 5 thru 7 are fast time plots of the PLL output, for complete Tevatron cycles, showing a continuous tune measurements. Comparisons with data from simultaneous measurements with a spectrum analyzer indicate that the system is capable of accuracy to $\pm .002$ (of fractional tune). The Tevatron Tune disturbances caused by the Main Ring accelerator magnet ramping are quite apparent in Fig. 6. The quality of the signals has a wide variation, depending on the mode of accelerator operation, and is not always sufficient to give this accuracy, or even a locked condition. In this application, vertical signal feedthrough on the horizontal signal (and vice-versa) is too close to be completely filtered out, and tends to pull the PLL off frequency, producing a measurement error.

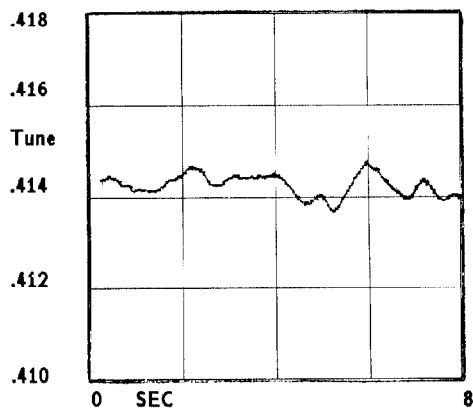


Fig.5 Plot of the Tevatron tune during collider operation.

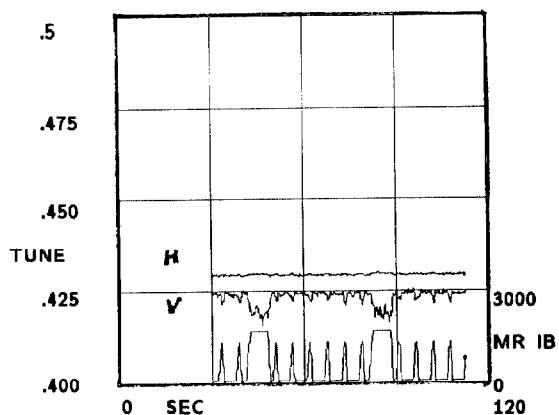


Fig. 6. Plot of the Tev. tune during fixed target run showing tune disturbances caused by the main ring bend current.

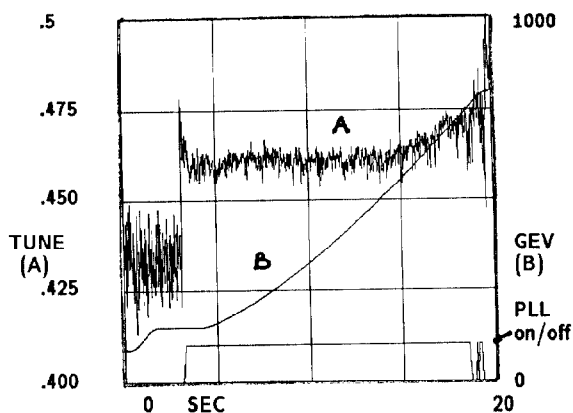


Fig. 7. Plot of the tune during fixed target run showing PLL locking and tracking during acceleration.

Conclusions

Because of the complex nature of the input signal, the high noise level, and the various harmonics and modulation present, a study of performance is highly statistical in nature. A phase-locked loop, connected as a tracking filter, will "lock" or center its VCO on the average of the frequency spectrum of the input signal, not necessarily the peak harmonic. The PLL will respond to all harmonics or FM noise in its tracking range, in accordance with their relative power content, as modified by the roll-off characteristics of the loop filter.

The measurement accuracy is therefore somewhat dependent on the signal to noise ratio and the symmetry of the input spectrum. In general, the accuracy of $\pm .002$ tune requires a signal that is at least 5 dB above a relative flat noise floor. Although it is by no means perfect, and has not replaced the spectrum analyzer, this system has shown to be a useful tool for measuring the tune.

The system is under continuing development, in an effort to improve its performance when the signal quality is poor. Testing has shown that the input conditioning circuit is not yet optimized. Under consideration is a narrow-band tracking-filter (adaptive filter), that has shown considerable improvement in isolating the peak signal. Future developments will also include an expanded system, that will provide the capability of beam excitation⁶ which greatly increases the detector signal strength when used.

References

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