A Frequency Tracking Synthesizer for Beam Diagnostic Systems

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Abstract

This paper describes a synthesizer scheme combining digital and analog synthesizer techniques to allow tracking of signals during acceleration. Virtually any ratio of synthesizer to beam revolution frequency may be generated by this scheme. Details of hardware and measurement results are presented.

I. INTRODUCTION

In low and medium energy synchrotrons the beam revolution frequency changes by a large factor during the acceleration process. High production rates require that these machines cycle rapidly. In attempting to diagnose instabilities which develop during the acceleration process it is useful to be able to select some frequency segment between revolution harmonics for viewing. Most types of test equipment operating in the frequency domain, such as spectrum analyzers and network analyzers, are not suited to making direct measurements on such rapidly sweeping signals. Ideally, one would want to set the frequency frame of reference to the spot in the accelerating revolution harmonic domain where the measurements are to be made. A scheme using a direct digital synthesizer (DDS) was developed to provide this moving reference frame.

II. THEORY OF OPERATION

The key to this tracking scheme is a DDS is used as an arbitrary ratio generator. Any type of frequency synthesizer and even digital divider circuits can be used to generate an output frequency which is proportional to the input frequency. For example, a phase locked loop (PLL) synthesizer generates an output which is related to the input clock frequency as

$$F_{out} = (F_{clock} * J) / K \qquad (1)$$

where J and K are integers, typically

$$1 \le J, K < 2^{16} .$$

Even though the frequency resolution of a PLL circuit would be sufficient for many applications, the main disadvantage for fine steps is the analog bandwidth of the loop filter must be proportionately narrow. This results in long settling times and frequency errors when attempting to lock to a rapidly sweeping clock frequency. The output phase noise of a PLL synthesizer increases if the loop is disturbed.

The DDS consists of digital adders, latches to hold the output of the adders, some type of sine conversion (a lookup table or algorithm), an output digital to analog convertor (DAC) connected to the most significant bits, and (usually) an analog low pass filter [1]. The system bandwidth is high and the total delay through the synthesizer is primarily due to the output filter. The close-in phase noise on the output of the DDS is equal to that of the input clock. The input digital word sets the phase accumulation per clock cycle and the rate at which the latch is clocked sets the phase update rate. Thus the output frequency is determined by the input digital word and the latch clock rate. The DDS output frequency can be expressed as

$$F_{out} = (F_{clock} * N) / 2^{M} \qquad (2)$$

where F_{clock} is the latch clock frequency and N is the digital input word value which can be any integer between 0 and $2^{M}-1$. M is 32 for most commercially available units. One can see that virtually any ratio of input to output frequencies can be created. The number of bits used in the output DAC determines the signal to spurious ratio (6 dB per bit). Low frequency DDS units typically use 12 bit DACs and high frequency units use 10 bit or 8 bit DACs. The primary limitation of the clock speed is the DAC. A practical limit to the output frequency of the DDS is roughly 0.4 times the clock rate. A low pass filter is required on the output to reduce clock harmonics and the upper image. This image frequency behaves as

$$F_{image} = F_{clock} - F_{out} \qquad (3)$$

Equ. 3 shows that as the input digital word value increases (causing an increase in output frequency for a given clock rate) the image frequency will decrease in frequency until the two signals eventually meet at half of the clock frequency. One could use this image frequency for driving test equipment if frequencies are needed above half the clock rate. Other methods

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of obtaining higher output frequencies are to use frequency multipliers before or after the DDS unit. These will be discussed in the next section.

The net result of this is if the input clock frequency is a harmonic of the beam revolution frequency then the output frequency will also track proportionally. One can set the digital input word of the DDS to the desired value and clock the unit from the accelerator RF system and generate signals which will track with the accelerating frequency domain.

III. HARDWARE IMPLEMENTATION

The initial test unit used a Qualcomm 2334 DDS evaluation board [2]. The DDS chip used has a maximum recommended clock rate of 50 MHz (although our particular unit runs fine up to 54 MHz) and the input frequency word is entered from a standard computer terminal through an RS-232 port on the board. A 10 bit DAC provides better than 60 dB signal to spurious ratio at the output. The evaluation board was designed for 30 MHz operation and therefore has a 12 MHz low pass filter installed. Most preliminary tests were done below this frequency.

Eventually it was desirable to generate frequencies above 12 MHz and so two external tripler circuits were added for higher frequency tests. The triplers tended to be difficult to align and the output contained many harmonics and sub-harmonics so a PLL output multiplier was used on later circuits. It is perfectly acceptable to use a PLL at this point in the circuit because the DDS has taken care of the fine resolution requirements and provides the PLL with a reference frequency of a few MHz. The PLL filter can be fairly broadband and thus will track the changing clock frequency very accurately. There is some degradation of output signal to noise ratio but it is still within the requirements of the system.

The various components required for the tracking synthesizer are incorporated into a printed circuit board version which uses an STEL-1375A DDS unit and a Qualcomm Q3036 PLL as the main components [3], [4]. Input buffers allow for frequency programming either from a 32 bit parallel input or from a microprocessor bus configuration. The PLL multiplier value is set using on board DIP switches. The board configuration allows for outputs to be generated directly from the DDS unit or from the PLL voltage controlled oscillator (VCO). For most of our applications the Motorola MC1648 VCO chip is adequate for the desired frequency range. Other commercial VCO units could be substituted for higher frequency operation [5]. A simplified block diagram of the tracking synthesizer board is shown in Fig. 1. Table 1 lists the synthesizer parameters. The addition of a multiplier (before or) after the DDS increases the minimum step size by the multiplication factor. In most cases this is not a problem. For example, using a 53 MHz clock rate the minimum step size out of the DDS is 12.3 milliHz. A multiplication factor of 81 would still give 1 Hz resolution.

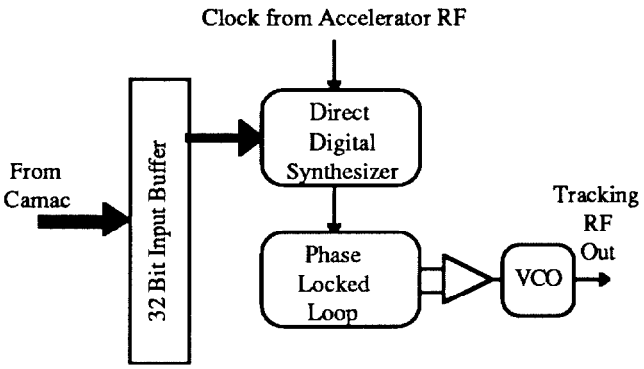


Fig. 1. Simplified block diagram of tracking synthesizer board.

Table 1
Tracking Synthesizer Parameters

Input frequency control	32 bit parallel or microprocessor bus
Maximum clock freq.	60 MHz
PLL multiplication	1 to 1295
Frequency resolution	1 part in 2^{32} / PLL factor
Output frequency range	DC to 24 MHz continuously, or octaves to 175 MHz (1.6 GHz with other VCOs)
Spurious outputs	< -55 dBc

An alternative to using a PLL or multiplier chain after the DDS unit would be to multiply the clock (by a factor of 20 or so) and use a much higher speed DDS unit. Commercial units are presently available with input clock rates up to 1 GHz [6], [7]. Advantages to this scheme are the need for only one multiplier design per accelerator and the ability to produce any desired output without changing circuit components. Disadvantages are the proportionally higher cost of the high speed DDS units and the limits to the DAC technology for output signal to noise ratio.

IV. APPLICATIONS

The tracking synthesizer scheme is used for studying coupled bunch modes in the Fermilab Booster [8]. In this installation the synthesizer provided the reference frequency for a network analyzer. Some pertinent Booster parameters are given in table 2.

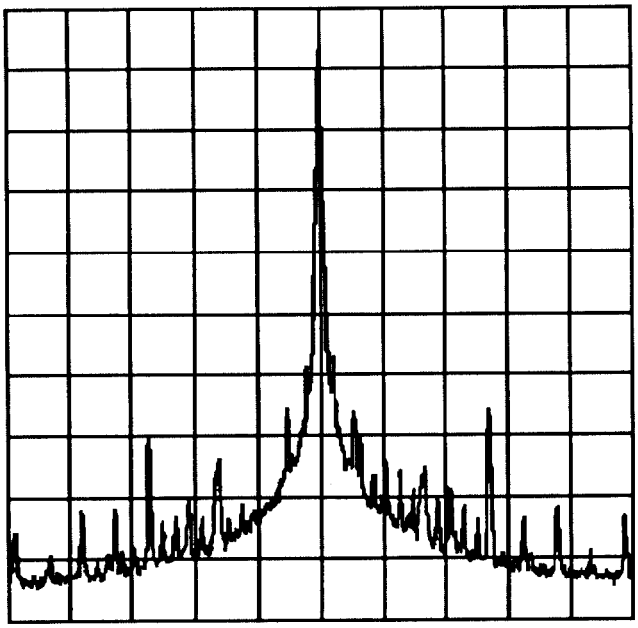
Since acceleration in the Fermilab Booster is dictated by the resonant characteristics of the magnets, the RF frequency is generated by a VCO which is in phase and radial position feedback loops.

Table 2
Fermilab Booster Parameters

Injection energy	200 MeV kinetic
Extraction energy	8.0 GeV kinetic
Circumference	474.2 meters
Cycle rate	15 Hz
RF frequency range	30.3 - 52.8 MHz
RF harmonic	84
Maximum frequency rate of change (@H=84)	5 GHz/sec

The magnetic field varies sinusoidally and therefore the RF frequency change is maximum near the beginning of the acceleration cycle. Also note that the frequency changes by a factor of 1.74 during the cycle. The tracking synthesizer works well for following such a rapidly changing signal.

Another installation which does not have nearly the slew rate requirements is the Tracking Emittance Monitor system in the Fermilab Antiproton source [9]. There the maximum frequency change is currently about 2.5% and occurs over a period of minutes for the E760 deceleration [10]. Fig. 2 shows the output spectrum from the tracking synthesizer for this installation.



Vertical = 10 dB/div. Horizontal = 100 kHz/div.
Center = 77.992 MHz.

Fig. 2. Output spectrum of tracking emittance monitor synthesizer board.

Future installations include general test oscillators and a longitudinal damper system for the Fermilab Booster [11].

V. CONCLUSION

A synthesizer scheme combining digital and analog synthesizer techniques to allow tracking of signals during acceleration is shown. This synthesizer makes use of the extremely fine frequency resolution of the DDS. It has been shown to track rapidly changing RF sources quite well and allowed measurements of various beam phenomena.

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