

# Prototype Studies of a 1 MHz Chopper for the KAON Factory

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## Abstract

A 1.025 MHz ( $\approx 10^6$  discrete pulses/s) beam chopper is required for the injection line into the Accumulator ring of the KAON Factory at TRIUMF [1]. The beam chopper will create 108 ns gaps in the 1 GeV/c  $H^-$  beam to allow enough time for the magnetic field to be established in the kicker magnets in each of the 5 rings. The required deflection of 1 mrad can be achieved with a set of plates 5 cm apart in which the product of voltage difference and plate length is 37.7 kV-m. The "kick" must have a rise and fall time of less than 39 ns and a flat top of 49 ns and 92 ns on alternate pulses. A novel design concept for a 1 MHz chopper has been developed involving an energy storage system where the electric pulses are stored in a large diameter (10 cm) low loss coaxial cable. Measurements on the performance of a high voltage prototype are presented. Results are encouraging and show that this novel design can be implemented successfully for the KAON Factory.

## I. INTRODUCTION

The TRIUMF cyclotron will be used as an injector for the KAON Factory synchrotron. The  $H^-$  beam pulse period is 43.5 ns, and allowing for jitter the effective beam burst width will be about 4.5 ns so that the effective gap between beam bursts will be about 39 ns [1]. The chopper rate will be 1.025 MHz with a 100% macro-duty factor with alternate pulse widths of 49 ns and 92 ns, as shown in Figure 1, so that 2 and 3 bunches will be removed alternately at approximately 1  $\mu$ sec intervals. Similar device at other laboratories operate at either low repetition rates in the 100 Hz range [2,3] or for example at a 0.25% macro-duty factor and 10 MHz [4]. The deflected beam bunches will impinge on a stripper foil and be further separated

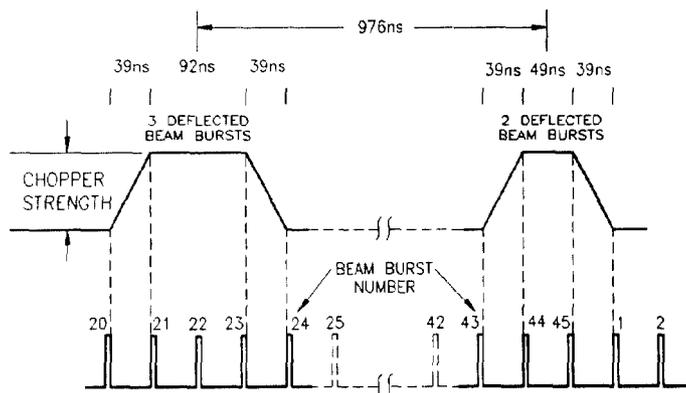


Figure 1: Pulse pattern of prototype 1 MHz chopper.

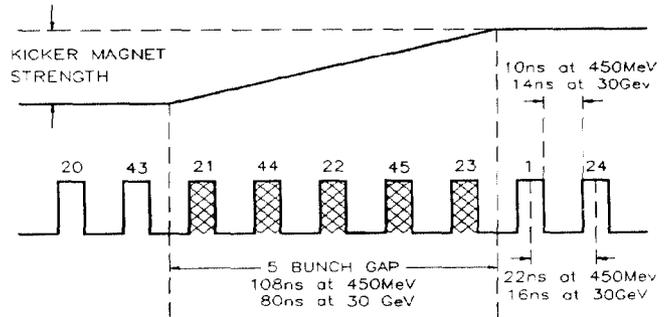


Figure 2: Beam burst pattern in the Kaon Factory rings.

from the undeflected  $H^-$  beam by a downstream dipole magnet and directed to a 10  $\mu$ amp beam dump. The accumulator ring will store  $H^-$  pulses in sets of 45, interleaved into two groups as shown in Figure 2 and the gap between most pulses will be reduced to 10 ns. The resultant gap for the kickers will be 108 ns in the accumulator ring with 5 consecutive bunches missing.

The rise and fall time of the driving voltage pulse ( $\tau_{v(r)}$ ), between  $a\%$  and  $b\%$ , and the propagation time ( $\tau_{beam}$ ) of the  $H^-$  beam through the center fed deflector plates must satisfy [9]:

$$\tau_{v(r)}^x + (M \times \tau_{beam})^x \leq (39 \text{ ns})^x \quad (1)$$

Where  $x$  is a power function and depends on the shape of the rising edge but is constant for fixed  $M (= \frac{b-a}{100})$ . If the pulse shape is trapezoidal then  $x \approx 1.6$  (2.1) for a 5%  $\rightarrow$  95% (10%  $\rightarrow$  90%) risetime [9]. If the deflector plates are 4 m long and the kick rise time is defined from 10%  $\rightarrow$  90%, then from equation (1) the rise time of the electrical pulse must be less than 38 ns.

## II. CHOPPER DESIGN CONCEPT

The original design concept has been described elsewhere [5,7,8] but has been modified somewhat and the present system will be outlined here. Electrical pulses will be stored in a very low loss coaxial cable that has a one way propagation time of approximately 1  $\mu$ s. This will permit the storage of two pulses of different widths that are 1  $\mu$ s apart.

### A. Original Design Concept

In the original design there were two tetrodes mounted at one end of a storage cable. The far end of the storage cable was connected to the center of a set of open circuit deflector plates which are configured as a 100  $\Omega$  stripline

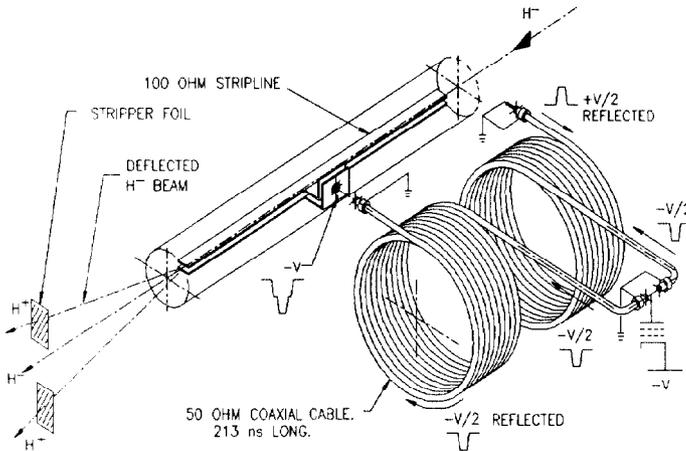


Figure 3: Prototype 1 MHz chopper

to match the impedance of the 50  $\Omega$  storage cable. The charger tetrode was used to reshape the leading edge of the stored pulse and the clipper tetrode was used to reshape the trailing edge of the pulse. The cable was connected to the charger tetrode at the cathode and to the clipper tetrode at the anode. The main disadvantage of this circuit was that the stray capacitance of the tetrode with the cathode connection was too high. The total stray capacitance in the prototype was about 1000 pF and it was not possible to achieve the required rise time. The best achieved rise and fall time of a 7 kV positive pulse was 65 ns and 90 ns respectively when both tetrodes were connected.

### B. Present Design Concept

The schematic for the present version of the KAON Factory chopper is shown in Figure 3. There is only one CY1172 [6] tetrode which is anode connected to the center of the storage cable. The total stray capacitance is about 240 pF. One end of the center fed cable is short circuited at the far end and the other end is open circuited. The cable is mounted to the tetrode in such a way that the inductance of the connection and the stray capacitance of the tetrode appears as a segment of lumped element 50  $\Omega$  transmission line. The inductance of the anode connection is shown in figure 4.

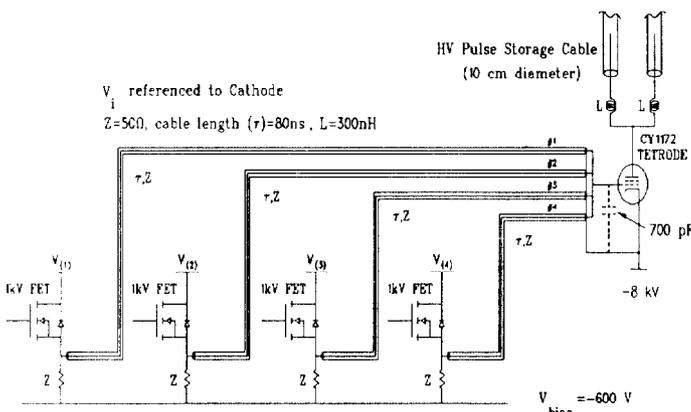


Figure 4: Prototype grid driver circuit for the 1 MHz chopper.

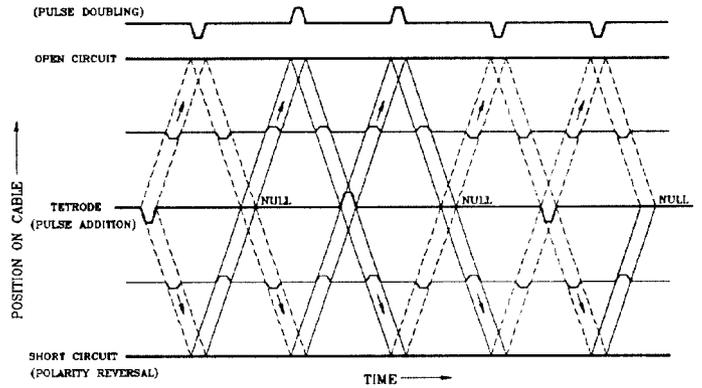


Figure 5: Lattice diagram of the 1 MHz chopper pulse pattern.

Figure 4 shows the output stage of the control grid driver circuit. The pulse pattern on each of the four parallel grid drivers was controlled through four fiber optic links from a pulse sequencer [11]. The pulse widths and amplitudes of each of the four fet pulsers could be controlled independently. The pulse sequencer permits operation with various burst lengths at macro-duty factors up to 100%.

Figure 5 shows the ideal pulse pattern at the center and at the open circuit end of the pulse storage cable. Each alternate reflection from the ends of the cable causes a null at the center of the cable. When the pulse at the center of the storage cable is negative the tetrode is turned on to restore the leading edge (charge). When the pulse at the center of the storage cable is positive the tetrode is turned on to restore the trailing edge (clip). The duration and the amplitude of the clipper pulse must be controlled very precisely to avoid overshoot or undershoot. The amplitude of the charge pulse is not so critical but the timing of this pulse relative to the storage cable length must be precisely controlled.

### III. PROTOTYPE TESTS

The prototype tests were carried out at about 2.3 MHz since the total available length of 10 cm diameter storage was 426 ns. The prototype deflector plates have not been connected to the system for any of the tests to date. If there were no stray capacitance or inductance then the pulse period at the end of the open circuit cable would be 426 ns. However the presence of stray inductance and capacitance introduces a delay. At a 3% macro-duty factor and a high voltage of 8 kV, the pulse period was varied until the fall time of the negative pulse was minimized. The best fall time occurred at a period of 436 ns (2.29 MHz). The free running period of pulses when the tetrode is turned off is 440 ns. Thus there is an effective phase shift of 4 ns every pulse period, between a driven edge of a pulse and the interpulse ripple. This turns out to be a significant advantage in eliminating the interpulse garbage. The interpulse garbage delays in phase for a few hundred pulses until it becomes absorbed into a high voltage pulse.

The pulse patterns shown in Figure 6 were measured 200  $\mu$ s after the first pulse at a 3 % macro-duty factor.

The solid (dashed) curves show the data for a wide (narrow) pulse pattern at the grid, anode and the open circuit end of the cable. The width of the anode pulse is determined by the relative delay of the grid clipper pulse. The amplitude of the pulses is about 7 kV and it can be seen that the null between the anode pulses is very clean. Table 1 shows a summary of the rise and fall times of the 4 measured voltage pulses at the open circuit end of the cable for the wide pulse pattern sequence shown in Figure 6. The deflection rise and fall times were calculated [9] for a set of 4 m deflector plates using the measured pulse patterns. The phase jitter shown in Table 1 relative to the first positive pulse and the ramp times must fit into the 39 ns gap between beam bursts.

Tests were also carried out at a 50% macro-duty factor and the pulse patterns were the same but the voltage levels were lower due to limitations in the power supplies. The power dissipation in the 150 kW tetrode was only about 7 kW at a 50% duty factor but the power dissipation in the grid pulser prevented operation above this rate. However the pulse repetition rate of 2.29 MHz is more than double the rate required for the final version so we were able to achieve  $1.14 \times 10^6$  pulses/s at about 6.5 kV continuously.

Table 1.  
Rise and fall times of wide pulses

Location of Pulse Edge	Voltage rise, fall (ns) 10%→90%	Deflection rise, fall (ns) 10%→90%	Phase Jitter $\Delta\phi$ (ns) $\pm 50\% \rightarrow \pm 50\%$
1 <sup>st</sup> pos			
Leading	14.7	18.2	0.0
Trailing	43.3	43.6	0.0
2 <sup>nd</sup> pos			
Leading	31	31.4	+6.2
Trailing	34.1	36.3	-6.8
1 <sup>st</sup> neg			
Leading	27.6	27.5	+9.5
Trailing	34.6	36.7	-6.7
2 <sup>nd</sup> neg			
Leading	16.2	19.4	-2.1
Trailing	38.5	39.9	+0.2

#### IV. CONCLUSIONS

The results show that the prototype chopper can achieve operation at 1 MHz continuously for 6.5 kV pulses and that we are very close to meeting the rise and fall time specification of 39 ns. Modifications are presently underway to further reduce the stray capacitance and inductance associated with the tetrode connection to reduce the ramp times and the phase jitter. The high voltage power supply is being replaced so that the chopper operate at 12 kV. The grid pulser is being improved so that we can achieve operation at 2.3 MHz continuously for the prototype tests.

#### V. REFERENCES

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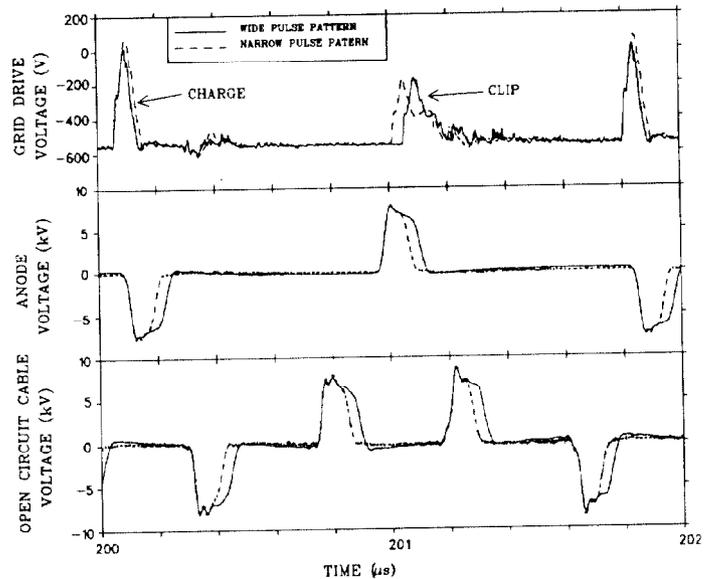


Figure 6: Measured pulse patterns on the grid, anode and end of the open circuit cable

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