Problems With Tap-Changing Power Supplies

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Abstract

To meet conflicting requirements for low ripple, high stability, wide bandwidth, high efficiency, and low radiated EMI, a synchrotron dipole power supply was built with an SCR tap-switched primary isolation transformer and linear bipolar transistor passbank. Numerous operational problems encountered after delivery and installation have necessitated a major overhaul of many of the supply's systems to meet full accelerator design goals. Particular emphasis is paid to the technique for switching taps on-the-fly for reliable operation.

I. INTRODUCTION

In October of 1983 the Indiana University Cyclotron Facility began construction of a 500 MeV electron cooled storage and acceleration ring. The ring is hexagonal in shape with six sets of dipoles. The dipoles placed a number of conflicting requirements on the power supply required to drive them:

1.) Low current ripple (5 mA @ 1650A)
2.) High DC current stability during fill and flattop (<10 PPM)
3.) Only moderate time constant of dipoles available for filtering voltage ripple (2.2 sec)
4.) Fast cycling (2-4 sec ramp from 45 to 500 MeV)
5.) "Reasonable" efficiency
6.) Restriction on the use of phase controlled SCRs due to close proximity of experimental equipment to power supplies (and consequent coupling of line noise into sensitive detector and beam monitoring sensors)

Dipole requirements were for 1650A and a peak load voltage of 185V at 500 MeV, 1 Tm/sec.

While a normal type of supply for this application would usually be an SCR phase controlled supply with damped LC filter and probably invert-to-the-line mode of operation, requirements 1.), 3.), 6.), and possibly 4.) would seem to work against such a topology. Consequently, a specification was written favoring the use of a linear bipolar transistor passbank and tap changed primary isolation transformer tapped for 70% (overwound), 100%, and 130% secondary output voltage that would be connected to the 600VAC line by back-to-back SCR pairs. A vendor was selected and the supply built, tested, and installed in the facility. A block diagram of the supply appears as Fig.1.

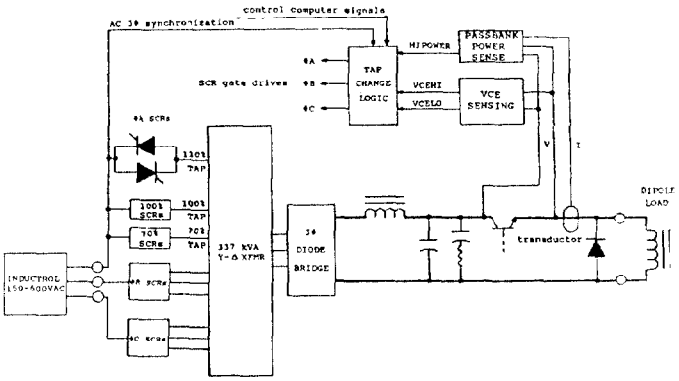

Figure 1. Tap-changing supply block diagram

Numerous problems were encountered in the first two years while the Cooler ring was being shaken down and commissioned. After inordinate expenditure of limited manpower resources in trying to keep the system operational and the fact that the supply could not reliably ramp beyond 287 MeV the decision was made in late 1989 to overhaul the entire tap-change scheme. The following sections recount progress in overcoming limitations of the supply and appear in rough chronological order; typically only one upgrade at a time was installed due to the tight running schedule.

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II. PASSBANK OVERPOWER PROTECTION

During the acceleration portion of an operating cycle the supply normally requires 130% (tap3) selection to provide inductive forcing voltage (Ldi/dt) to the load. As the ramp begins to round off and head into flattop the load voltage drops rapidly; excess voltage from being on tap3 is now forced across the passbank until the supply can fully complete a downshift to 100% (tap2), initiated by either VCEHI or HIPOWER (Fig.1) in conjunction with the external computer command allowing it to start the downshift. Timing here becomes quite critical as the passbank DC dissipation limit is only 70 kW and passbank power levels can easily exceed 100 kW while waiting to downshift.

To overcome these deficiencies a passbank power monitor board was constructed to closely model the second-breakdown portion of the D60T passbank power transistors. Computed power is determined by multiplying collector current and passbank voltage. This is then fed to an RC network to do a first-order approximation of the transistor hot-spot temperature. This signal then feeds a comparator that shuts off drive to the tap-change SCRs in the event of overpower. Raw DC collapses within 10 msec and the passbank power stress is relieved. To backup this primary overpower system two slower overpower interlocks from the existing systems function to drop out the main contactor. While previous overpower events had destroyed transistors by the dozens we have now completed two years of running with no further transistor failures.

III. TAP CHANGE SCHEME

Originally the supply was intended to initiate tap changes based on both internal status signals (VCEHI, VCELO, and HIPOWER) and external control computer signals (to prevent tap changing while not ramping). Operationally there were territorial disputes from this combined hardware/software tap change scheme. The upgrade called for only internally triggered switching to be used. Also, to make use of only internal trigger signals a series of tests determined that tap changes would have to execute in less than 50 msec in order to avoid overpower trips.

Because the existing tap change scheme did not directly sense SCR status, occasionally blown SCR fuses would result from multiply energized taps, causing several hours of downtime to replace. In the upgraded tap change logic, SCR ON/OFF sense would be determined by either SCR anode current sensing or SCR anode-cathode voltage sensing. Pros and cons for the two approaches are shown in Table 1:

Table 1
SCR ON/OFF sensing

Method	Pro	Con
Current sensing	*low cost, simple	*poor signal-to-noise ratio *not inherently failsafe
Voltage sensing	*good signal-to-noise ratio over many decades of SCR current *failsafe	*complex

The degree of "failsafeness" refers to whether the system would allow a tap change in the event of typical component failures; bad CTs, broken connectors and so on would give a "no current, OFF" status allowing a new tap to be loaded while an existing tap was still energized. Similar failures with voltage sensing (bad PTs, broken connectors, etc.) would give a "no voltage, ON" status and inhibit new tap loads; at worst a phase imbalance interlock would occur as opposed to SCR fuse failures. A block diagram of the tap change technique appears as Fig. 2. Because we were not interested in precise values of SCR anode-cathode voltages (anything over 15 volts was considered OFF) a series of inexpensive 50VA 600/120V machine tool control transformers were used as SCR potential transformers.

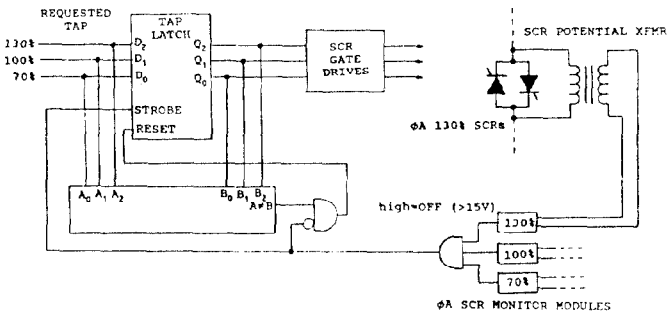

Figure 2. Tap change technique (phase A)

Results after 8 months of running have validated the usefulness of the technique. No further SCR fuse failures have occurred while ramping to record energies for the ring (485 MeV) in numerous runs. As expected, tap changes are fast (10msec) and are clean step changes up and down. Because of the immediate success of the technique, further side effects of the tap-changing approach became apparent above the former 287 MeV supply limit.

IV. SUPPLY RESPONSE TO UNREGULATED DC STEP CHANGES

Filter Damping

Ringing of the input filter on tap changes leads to small undershoots in the unregulated DC. For lower energy ramps (< 287 MeV) these could be tolerated by setting the AC input voltage slightly high by using the inductrol in Fig. 1. For higher energy ramps, power constraints rule out this technique and as a consequence transient saturation of the passbank occurs, leading to output glitches. Simply increasing the filter damping was not an option as ripple (which was already considered high) would increase with increasing filter damping.

After modeling the input filter in SPICE and exploring several impractical non-linear filter damping resistor options (e.g., PTC thermistor arrays) a two-state variable damping filter modification was decided upon; this is shown in Fig. 3.

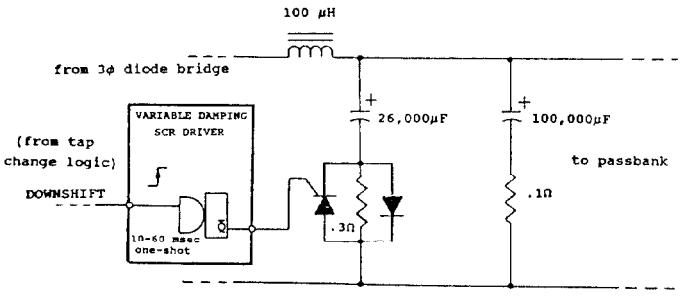

Figure 3. Filter variable damping

During normal operation the SCR around the damping resistor is ON and, in conjunction with the anti-parallel diode, provides a short-circuit for capacitor ripple currents. When a downshift occurs the SCR gate drive is turned off momentarily (10-60 msec), the SCR commutates and the normal large reverse ring current out of the filter is reduced greatly due to the sudden "appearance" of the .3 ohm resistor. Damping is such that no undershoot now appears; the supply does not lose regulation and normal steady-state ripple is unchanged.

Passbank Oscillations

The final roadblock to 500 MeV operation proved to be troublesome passbank internal oscillations. Due to the high f_t of the D60T transistors, the sudden rise in passbank voltage when going into magnet reset (current drops from 1600A to 250A) causes a shock-induced oscillation of the passbank at several kilohertz. This was eliminated (after numerous false starts) by using a distributed capacitive bypassing of the collector to minus bus scheme.

V. TAP OSCILLATION DETECTION; FORBIDDEN RAMPS

An anticipated result of using only internal signals to control tap changing is that in certain instances it may not be possible to find a stable operating point (given a desired ramp rate, flattop, and inductrol setting) where passbank voltage is sufficient but passbank power is not excessive. In these instances of "forbidden ramps" the supply will enter a steady-state oscillation mode trying to switch rapidly between taps to satisfy both conditions; damage to magnetic components, filter capacitors, and switchgear could result if this continued.

To prevent damage a tap oscillation detector looks at the 100% tap (since any oscillations must involve this middle tap) and shuts down the supply if more than a minimum number of tap changes occurs in an adjustable timeout period (typically 1 sec). This circuit has also proved useful in preventing damage from high-order dropped bits in the DAC. The resulting sawtooth waveform from the DAC would normally cause a rapidly tap-changing supply situation and consequent supply damage. A block diagram of this circuit is shown in Fig.4.

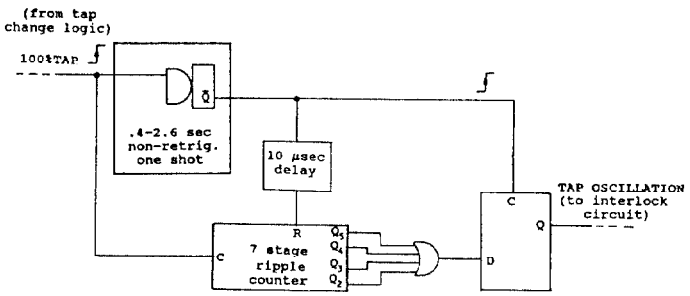

Figure 4. Tap oscillation detector

VI. SUMMARY

With sufficient justification it is possible to produce reliable tap-switched power supplies to meet multi-kilowatt load requirements. The justification (given the supply complexity) is rather limited to special combinations of requirements in cases demanding:

*high bandwidth for small ramp following errors
*moderate time constant loads where the load itself provides insufficient ripple current attenuation so that an active filter is necessary
*need exists to minimize line noise, equipment size, energy costs
*high DC current stability with minimum AC ripple