# Amplitude and Phase Regulation of the RF Separator

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### Abstract

The RF separator at TRIUMF has the cavity located 20 m from the power amplifier. This system is controlled by analog regulators with programmable loop parameters. The controller hardware is modular and can easily be adapted to other RF systems at TRIUMF.

### Introduction

The separator is used to produce a negative muon beam in the TRIUMF M9 secondary beam line.[1] Pions and electrons are suppressed to less than 1% of the beam by crossed magnetic and electric fields in an RF cavity. The cavity is driven at the main cyclotron frequency (23 MHz) and phase locked to the primary proton beam.

The original regulator was based on a digital controller which had a minimum loop delay of 150 us. This is longer than the cavity time constant of 70 us and it places the principal system pole near the origin in the Z domain. With such an arrangement, one can achieve a reasonable servo response where the output reaches its target value in a number of sample periods equal to the order of the system. However the RF system, including the cavity and power amplifier, had a disturbance spectrum which exceeded the bandwidth of this controller. It was decided to rebuild the separator RF system and, as part of this effort, the regulator was changed to an analog design.

This provided an opportunity to install a new, modular RF controller.[2] The task in developing such a system is to identify the basic discrete functions and build a hardware module to perform only that function. Complex systems can then be pieced together from these basic elements. Simple, basic elements are also easy to change or upgrade. However, if a single device becomes too specialized or complicated then it may become an orphan, useful only in one specific installation. It is hoped that several RF systems can be assembled from the basic elements that are identified in the separator design.

An on board computer provides manual and remote access to the controller. It also handles graphic display of the system variables on the front panel and sequencing for automatic start up and spark recovery. The computer facilitates the development of modular display and sequencing hardware. The main disadvantages are:

- The RF group must identify individual software modules that can be assembled into other RF systems.
- Computers are an evolving technology that is subject to change and even revolution every few years.

### Description

The computer software for automatic sequencing and system I/O was developed on IBM PC compatible computers. The IBM PC environment offered several advantages in that the available languages have been debugged by a large user base. The compilers are well supported, easy to use and most have the graphics and timer support needed to produce the bar graphs, system pictorials and sequencing operations. A simple polling loop is sufficient to handle the controller I/O.

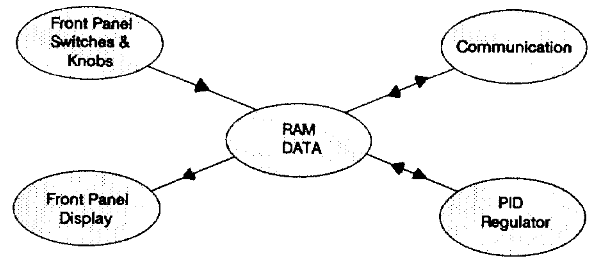


*Fig. 1 Controller I/O Tasks*

The prototype controller was built using a 7 MHz PC on STD bus with Prolog's System 2 operating system. The installation performed well and could easily handle the necessary tasks however the STD packaging is not well suited for shielding individual printed circuit boards in an RF environment. Work is under way to base the system on a 10 MHz AT in VME bus. It is felt that this has several advantages:

- most other labs use VME hardware.
- VME offers RF shielded packaging.
- if desired, the computer group can rewrite the software for a different processor and display.

A gas discharge plasma display is used as the front panel display. It is compatible with IBM's EGA graphics but unlike a CRT, it is not sensitive to magnetic fields or phosphor burn. The front panel information is shown in Fig. 2.

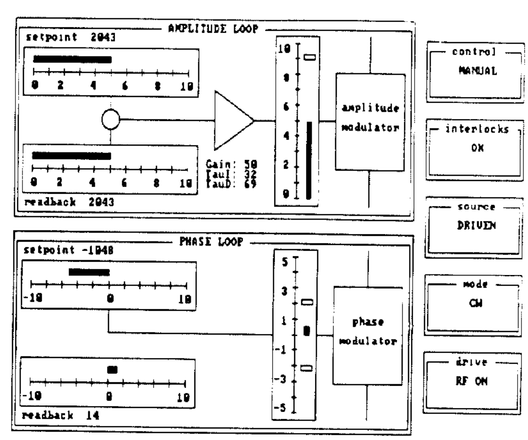


*Fig. 2. Front Panel Display*

The amplitude and phase regulators can operate in closed loop or open loop. The display indicates the state of each loop. Set point and readback values are displayed numerically and with horizontal bar graphs. The modulator drive signal and an adjustable drive limit value are displayed with the vertical bar graph. System status is shown at the left side of the plasma panel.

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Push buttons on the front panel are used to change system states such as RF On/Off, Open/Closed loop etc. Continuous parameters are changed using five optical shaft encoders on the front panel. Two of the shaft encoders can be assigned to adjust either the regulator gain, pole cancellation, or the drive limit for each loop. The remaining three knobs are dedicated for amplitude and phase set points and the RF pulser duty cycle. The assignable knobs are used mainly during setup and commissioning while the dedicated knobs are used in regular operation. Keeping multiple assignments to a minimum reduces the complexity of the front panel controls.

Whenever possible, commercial peripheral cards are used in the controller. However, more hardware resources were available than were software and programming expertise. Three peripheral cards were built for the computer bus. Two of these serve to simplify the program. One card allows the computer to read the front panel knobs and push buttons. When a button is pushed or a knob turned, the event sets a single bit in one of two 8 bit registers. The hardware automatically resets these registers at the end of a read cycle. The polling loop need only read the registers and take appropriate action if they are non zero.

The RF is pulsed during startup to overcome multipactoring in the resonator. A second peripheral card was built to handle this operation. The computer writes the pulser frequency and duty cycle to registers on this card.

A block diagram of the analog regulator is shown in Fig. 3. It is a basic PID configuration. Multiplying DACs are used to implement variable gain elements that allow independent control of the loop gain, K and the time constants T1 and T2. The regulator zeros can be placed between 300 Hz and 200 KHz and the gain control has a range of 70 db, similar to a $(PI)^2$ regulator built by L. Durieu.[3] A 12 bit DAC is used to control the set point and an on-board ADC monitors the drive level and detector output. The switch changes the control between open loop and closed loop.

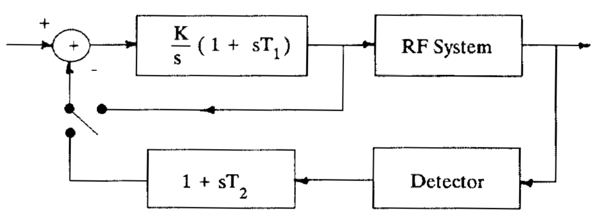


*Fig. 3 Regulator Block Diagram*

The regulator boards used with the VME system are in double height VME format (6U). The top connector conforms to the VME J1 standard while the only outside rows of the P2 connector are used to connect analog signals to the regulator. Pins on the P2 connector are not bussed. Instead they are connected directly to the appropriate loop elements. This configuration allows us to take advantage of commercial VME packaging and hardware. The signal paths between the computer and the regulator electronics are optically isolated to eliminate ground loop problems. [2,4] Figure 4 shows the regulator board format.

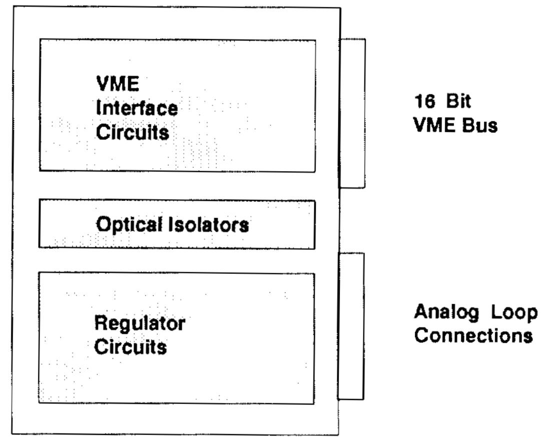


*Fig. 4 Regulator Card Format*

## Operation

When testing the regulator, the drive limiter and the ability to switch easily between open and closed loop proved to be very useful. The limiter was suggested by the RF group at SIN in Villigen, Switzerland.

The RF systems at TRIUMF operate CW. Independent control of the loop gain and pole cancellation allows the loop to be quickly tuned in the frequency domain. It is easy to determine the gain-bandwidth trade off with respect to rejection of the system disturbance spectrum. The wide tuning range allows one to stabilize a loop with almost no prior knowledge of the system or its delays.

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