DESIGN AND IMPLEMENTATION OF A VMEbus SYSTEM SERVICES CARD

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Introduction

The System Services Card (SSC) is a multi-function VMEbus module designed to provide useful debugging features for code development and system services that are needed in most configurations. The card has the following features:

- 80 character by 24 line composite video signal (6845 CRT controller)
- Two serial I/O ports (68661 and 68901)
- Time of day and date with alarm clock (Dallas Semiconductor DS1286)
- Slot 1 System Controller (Mizar VME 1000)
- Four 8 bit timers (68901)
- System reset watchdog timer
- Five front panel 5X7 dot matrix displays
- Software readable up/down counter with front panel control
- Front panel LED display with test points (32 bits)
- Front panel DIP switch (8 bits)
- Front panel push button bit set with interrupts (2 bits)
- Circuit board DIP switches - software readable (32 bits)
- General Purpose I/O (8 bits)
- Front panel system reset button
- VMEbus interrupts from on-board devices
- Eight channel interrupt generator for inter-processor communications
- Audio alarm

General Description

The System Services Card is a single width VMEbus module that occupies 4 Kbytes of memory in short I/O space. A four position DIP switch on the circuit board is used to position the SSC on any 4 Kbyte boundary. The 4K used by the SSC is divided into two equal sections. The first is used for the video display and the second half is used to address all of the other devices on the card.

Most of the devices on the module are 8 bits and for these the card functions as a D8(EO) slave. Two of the functions, the 32 bit LED display and the 32 bits of readable DIP switches, can be accessed with bytes, words, or long words. For these, the module functions as a D32, D16, or D8(EO) slave.

In addition to providing a variety of I/O devices, the System Services Card can function as a slot 1 system controller with several bus arbitration options, and it has an 8 channel interrupt generator that is intended for use in inter-processor communications.

A complete software support library is currently being written to provide a high level language interface to the card. These routines allow the use of multiple cards within a single VMEbus crate. The library provides routines to access all devices on the SSC. A description of each of the features on the module is given below. Fig. 1 shows those features that are provided on the front panel.

Video Output

The System Services Card outputs a composite 80 character by 24 line video signal from both a Lemo connector on the front panel and from the rear J2 connector. The video RAM appears as a 2K block of byte addressable RAM in the first half of the 4K block occupied by the card. ASCII characters written into the video RAM are displayed on the video display. In addition to ASCII text, 64 codes have been converted into graphics characters. These characters convert the screen from the normal 80 X 24 text mode to a 160 X 72 graphics mode. Text and graphics can be mixed to produce a variety of graphical effects including rectangles and ovals used for highlighting text and building graphs, and bar charts. The character set is fixed in EPROM but can be changed for special situations. The video controller for the display is the Motorola 6845 which appears as a group of 8 bit registers within the second half of the 4K memory map.

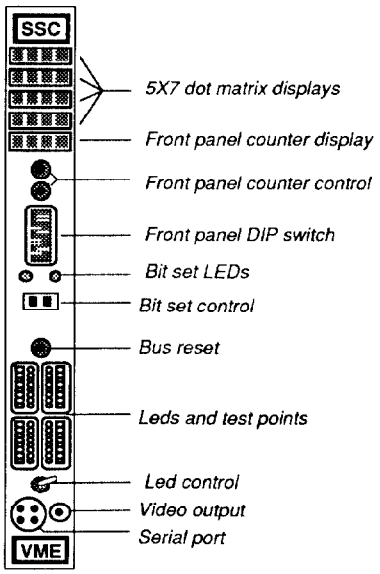

Fig.1 Front panel view of the System Services Card

RS 232 I/O

Two serial ports are provided on the SSC. The primary port is based on the Motorola Enhanced Programmable Communications Interface (68661) and is brought to the rear J2 connector the of the module. The 68661 can be operated either synchronously or asynchronously. It contains a baud rate generator with 16 different baud rates which are selected under program control. The port has a set of jumper options on the PCB that are used to configure the port as either data terminal equipment (DTE) or as data communications equipment (DCE). Three output signals from the 68661, Transmitter Ready, Receiver Ready, and Transmitter Empty/Status Change can be used to generate VMEbus interrupts through the interrupt controller in the 68901 multi-function peripheral.

The second serial port is based on the 68901 which is also used to provide a number of other features on the module. This port is wired to a front panel connector and is intended to drive a portable terminal. The baud rate generator for the port is separate from that of the first port and is also programmable. The port can generate interrupts for transmitter buffer empty, transmitter error, receiver buffer empty, and receiver error using the internal 68901 interrupt structure.

Time of Day and Date

The Dallas Semiconductor DS1286 is used on the SSC to provide time of day and date information to the system. The device

* Operated by Universities Research Association, Inc. under contract with the U.S. Department of Energy.

keeps track of hundredths of seconds, seconds, minutes, hours, days, day of the month, months, and years. The device appears as a block of sixty four 8 bit registers in the I/O space of the card. Of these, only 14 are used for the time keeping functions; the rest are available for general purpose use. The device has its own power backup that maintains all functions of the chip in the absence of VCC. The device has an alarm function which can be used to cause interrupts at a preset time, or once each day, or hour, or minute.

Slot 1 Controller

The System Services Card can be used as a slot 1 system controller. Functions supported include the VMEbus arbiter, an IACK daisy-chain driver, a 16 MHz SYSCLK driver, a Bus Timer, an Arbitration Timer, and a SYSRESET* driver.

The SSC supports all three arbitration modes defined in the VMEbus specification: Priority (PRI), Round-Robin-Select (RRS), as well as Single (SGL). When operating in the PRI mode, the arbiter asserts the BCLR* line whenever it detects a request for the bus whose level is higher than the one being serviced. In RRS mode, BCLR* is asserted whenever a bus request is received on a bus level other than the level currently granted the bus.

The Bus Timer on the SSC asserts BERR* if either DS0* or DS1* is maintained in the active state for longer than 64 microseconds.

The Arbitration Timer on the SSC asserts BERR* if no master asserts BBSY* within 16 microseconds after the arbiter has granted the bus to a requestor. This allows the system to recover from a hanging bus grant.

The SSC has a global reset driver which provides a system reset by asserting the VMEbus signal SYSRESET*. This signal is asserted at power up and by a push-button switch on the front panel. A jumper is provided on the circuit board to disable the switch. SYSRESET* will remain asserted for at least 200 milliseconds as required by the VMEbus specification.

In addition to the jumper to disable the manual SYSRESET* switch, there is a jumper on the circuit board to disable the remaining slot 1 functions. There is also an input to the card to externally trigger the SYSRESET* signal and another input to inhibit the same signal.

Timers

The Motorola 68901 Multi-function Peripheral contains four 8 bit timers. All four timers run from a common time base of 1 MHz, however, each of the timers has a pre-scaler. The pre-scaler divide ratios are 4, 10, 16, 50, 64, 100, and 200. All of the timers can be read during the timing period.

Two of the timers have a single mode of operation while the remaining timers have 2 additional counting modes. The delay mode, which is common to all four timers, has the timer count down to zero from a pre-loaded value when enabled by software command. An interrupt is generated when the counter reaches zero. Also, at zero, the counter reloads to its preset value and begins counting down again. This process continues until the counter is disabled with a software command.

The additional counting modes available on two of the timers are the pulse width mode and the event count mode. The pulse width mode uses an extra auxiliary input to the counter to gate the counter on and off. Pulse width measurements are made by determining the number of counts recorded during the time that the counter is enabled by the external gate signal.

The event count mode makes use of the same extra input to the counter as in the pulse width mode. In this mode, the pre-scaler is disabled, allowing each active transition on the extra input to produce a count pulse. The number of events that have occurred is determined by examining the contents of the counter.

The outputs of all four counters are brought to the rear J2 connector as are the extra inputs of the two multi-function timers. The outputs of all counters toggle to the opposite state whenever the counters reach zero. This produces square waves at the outputs with periods twice that of the countdown periods.

System Watchdog Timer

The system watchdog timer on the SSC is a two stage circuit designed to simplify the task of retriggering the watchdog during the time that code is being downloaded to the system. The first stage has the normal time-out period and resets the bus if the watchdog is not periodically retriggered. The second stage has an additional time-out period that must elapse before the watchdog is reactivated. Both time periods are DIP switch programmable to accommodate various system requirements. The time base for the first stage of the watchdog is .01 second, giving a time period of from .01 to 2 seconds. The time base for the second stage is 10 seconds, giving a delay of from 10 to 2,000 seconds before the watchdog again becomes active. The watchdog timer may be disabled with a jumper option on the circuit board.

Dot Matrix Displays

The front panel has 5 programmable character displays. Each display is 4 characters wide and each character is a 5X7 dot matrix. The fifth display serves two functions. It can be programmed to display the contents of the up/down counter described in the next section or it can be used simply as another display like the other four.

In the interest of flexibility, each dot of each display is individually addressable. This allows the displays to be used for more than just ASCII text. The displays are used to provide visual information on a variety of processes within the VME system. For text display, software routines have been written that shield the user from the complexity of the individually addressable dots.

The bit map for the displays is a 256 byte block of memory. Four of these blocks are provided in a 1 Kbyte RAM. The displays can be switched between the four bit maps under software control.

Readable Up/Down Counter

The module has a software readable up/down counter. The contents of this counter can be displayed on the 5th dot matrix display discussed in the section above. The counter is 8 bits (00-$FF).

The direction of counting is controlled by two push buttons located on the front panel. Each push of the appropriate button will increment or decrement the counter by one count. Depressing a button for longer than half a second will fast forward or reverse the counter. The buttons can be disabled with a jumper option on the circuit board. Another jumper option causes an interrupt to be generated on the VMEbus each time the counter is incremented or decremented. The contents of the counter can be read as a byte only.

LED Display

The front panel has four groups of 8 LEDs and test points. The LEDs are controlled by the contents of a 32 bit read/write register on the card. Any bit loaded with a "1" will light the corresponding LED. The outputs of the 32 bit register do not directly drive the LEDs. Rather, each LED is driven by a one shot circuit that will light the LED for some minimum time (to make it visible) but will also keep the LED on longer if the corresponding bit in the register remains set.

The one shot circuit is triggered by the low to high transition of the corresponding bit in the register. Thus, short duration sets of the bits of the register are made visible by the one-shots, while DC conditions are also displayed. There is a single timing adjustment potentiometer on the circuit board to change the timing periods for all the one-shots. The adjustment provides a timing range of from .1 to 5 seconds. A switch on the front panel allows the one-shots to

be bypassed completely if desired. This same switch has a center position that functions as a lamp test for the LEDs.

The 32 bit register can be accessed in bytes, words, or as a single long word.

Front Panel DIP Switch

An 8 bit DIP switch that can be read as a register in I/O space is mounted so that it is accessible from the front panel. The register can be read as a byte only.

Push Button Bit Set

Two identical bit set circuits are provided, each with push button control from the front panel. Each of these circuits toggles the MSB of an 8 bit read/write register when the corresponding button is pushed. The registers are accessed as bytes but only the most significant bit is meaningful. When either of the bits is set, it will remain set until the flip-flop is reset by software or until the corresponding button is pushed again. A flip-flop is reset by writing a "0" to the b7 bit of the latch. Each of the push buttons has a jumper on the circuit board that enables or disables the button. The outputs of the one bit registers may be selected as sources of interrupts on the VMEbus. Two LEDs on the front panel show the states of the bits.

Readable DIP Switches

Four 8 bit DIP switches on the circuit board are readable as a 32 bit register in the I/O space of the card. The register supports byte, word, or long word reads. These switches are used to convey system information to the bus processor at power-up.

General Purpose I/O

The 68901 multi-function peripheral includes 8 general purpose I/O lines. These lines, which can be individually programmed to be inputs or outputs, are routed to the rear J2 connector of the SSC. As inputs, these lines are high impedance receivers and as outputs they are TTL compatible. When programmed as inputs, the lines can be enabled to act as sources of interrupts, each with its own interrupt vector. The active edge for triggering interrupts is also individually programmable.

Besides going to the J2 connector, the eight I/O lines are routed to jumpers which allow the lines to be used to generate interrupts from several other on-board devices. These devices include the 68661 serial port, the alarm clock feature of the DS1286 day/date chip, the 2 manual bit set push buttons, and the software readable up/down counter. Those lines which are selected to cause interrupts from on-board devices cannot be used to input signals from the J2 connector.

Interrupts

The SSC can generate interrupts on the VMEbus from a total of 24 different sources. Sixteen of these interrupts are generated through the 68901 multi-function peripheral device while the remaining 8 interrupts are generated under software control using a pair of 68153 interrupt generators.

68901 Interrupts

Eight of the 16 interrupts generated by the 68901 multi-function chip are generated by functions contained in the 68901 itself, while the remaining interrupts are caused by activity on the 8 I/O lines of the device. The 68901 has a single IRQ output line which can be jumper connected to any of the VMEbus IRQ1*-IRQ7* interrupt lines. The 68901 will return a separate vector for each of the 16 possible interrupt sources whenever it responds to an interrupt acknowledge cycle on the bus. A list of the interrupt sources in order of priority from highest to lowest is given below. The items in parenthesis are the on-board devices discussed in the previous section which can be selected with jumpers to replace input signals coming from the J2 connector.

General Purpose Input 7 (alarm clock output A)
General Purpose Input 6 (up/down counter change)
Timer A
Receiver Buffer Full
Receive Error
Transmit Buffer Empty
Transmit Error
Timer B
General Purpose Input 5 (push button bit set #1)
General Purpose Input 4 (push button bit set #2)
Timer C
Timer D
General Purpose Input 3 (alarm clock output B)
General Purpose Input 2 (68661 TxRDY output)
General Purpose Input 1 (68661 RxRDY output)
General Purpose Input 0 (68661 TxEMT/DSCHG output)

Interrupts for Inter-Processor Communications

The SSC has a pair of 68153 Interrupt Generator devices that are used to generate VMEbus interrupts under software control. Each device has 4 interrupt channels that can individually be programmed to select the interrupt level (IRQ1*-IRQ7*) that the channel uses and the vector that the channel returns when the interrupt is acknowledged. Once programmed, a channel can be triggered to initiate an interrupt by writing to an interrupt register on the card. In this way inter-processor communications is implemented by allowing any processor to generate an interrupt on any level and to provide a programmable vector during the interrupt acknowledge cycle.

Audio Alarm

A simple beeper has been included on the SSC. The beeper is triggered by writing to a specific address on the module. The beeper sounds for approximately one half second each time it is triggered.

Conclusion

The System Services Card was designed by both hardware and software persons to provide a wide range of services for VMEbus computers at Fermilab. The object was to consolodate into a single card many of the functions that are now scattered over serveral cards or are not provided at all. A high priority was put on providing a number of simple but useful interfaces between the programmer and the hardware to simplify code debugging. Most of the functions on the SSC have been tested in prototype form. The printed circuit board for the module is currently being routed with production units scheduled for testing in June '89.

Acknowledgments

The authors wish to acknowledge the following people for their design contributions toward this module: D. Dupuis (front panel and PCB design), D. Horch (watchdog timer, dot matrix display, up/down counter), C. McClure (bit set interrupts, inter-processor interrupts, audio alarm), J. Ticku (video display, slot 1 controller, address decoding), and J. Utterback (software routines for user interface and prototype debugging).