Vax Q-Bus to CAMAC Systems Crate Interface for Long Camac Branches

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Abstract

The TRIUMF Central Control System (CCS) was to be upgraded to use Q-Bus based Vaxes. The CCS consists of multiple computers interfaced to a CAMAC Executive Crate with long parallel branches containing multiple pairs of Differential Branch Extenders (DBE). The Creative Electronics System SCI 2280 systems crate interface used for the Q-Bus Vax requires the CAMAC operation to complete synchronously with the Q-Bus cycle in less than the Q-Bus timeout period. This translates to a maximum branch length of about 150 meters containing 3 pairs of DBEs, which was not adequate. A Q-Bus to SCI 2280 interface was built to allow CAMAC cycles to be decoupled, when desired, from the Q-Bus cycles. When cycles are decoupled, completion of the CAMAC part can be ascertained by testing flags in the interface. A description of the interface design and its operation as well as the results of tests using a VAX 3500 will be given.

Introduction

The TRIUMF Central Control System is a CAMAC based system consisting of Data General computers connected through a Fisher Executive Crate to seven parallel branch highways. From the branch couplers some parallel highways extend more than 150 meters through Joerger Differential Branch Extenders to type A2 CAMAC crate controllers. The introduction of DEC Q-Bus based computers [1] and the CES SCI 2280 System Crate Interface into the control system at the executive crate level revealed a timeout problem on the long branches. CAMAC commands go from the VAX through the SCI 2280 and a branch coupler module. The reply from the CAMAC crate arrrived after an internal 10.5 μS timer in the DEC computer expired resulting in an incomplete cycle error. This system problem limits the use of the Q-Bus based VAXs to shorter branches.

The 10.5 μS timeout is implemented in the VAX microcode and is not accessible to the user. Attempts to solve the problem by modifying the SCI 2280 to operate in a polled or non-transparent mode were unsuccessful. Since the problem originates with the VAX the solution must let the VAX complete its memory cycle within the timeout period but let the cycle continue to completion in the CAMAC environment. A new device was required in the executive crate to replace the SCI 2280 or in the VAX to interface with the existing SCI 2280. The interface within the VAX was clearly the simpler of the two options.

System Description

The TRIUMF 0715 module allows VAX timing to be independent of CAMAC operation timing. Before considering the role of the 0715 we examine normal VAX to SCI 2280 operations. The SCI 2280 [2] is a memory-mapped device in VAX address space. The VAX loads CSR bits 12-8 with the Branch and Crate fields and loads bits 4-0 with the N or F field of the CAMAC address. Jumpers in the SCI 2280 determine whether CSR bits 4-0 are interpreted as the N or F field of the CAMAC address. Assume the CSR contains the N field. A 24-bit CAMAC write operation is executed by writing bits 24-17 into the DBH register in the SCI 2280 then writing bits 16-1 to an address which encodes the A and F fields as an offset from a base address. The SCI 2280 interprets this address plus the B,C and N fields in the CSR as the CAMAC operation to be executed using the data in the DBH register plus the data on the Q-Bus lines. The Q and X returned from the CAMAC operation are saved in CSR bits 15 and 7. The CSR is read by the VAX to get the Q and X responses. A similar sequence occurs for a CAMAC read operation. The VAX loads the CSR with the B,C and N fields then reads from a memory address which encodes the A and F fields. The result of the memory read are CAMAC data bits 16-1. Bits 24-17 are saved in the SCI 2280 DATA_BYTE_HIGH (DBH) register. The VAX then reads the DBH register to get bits 24-17 and reads the CSR to get Q and X.

When the 0715 interface is added to the system the sequence is modified as shown in Figure 1. Consider a CAMAC write operation. The VAX loads the B,C and N fields into the CSR then loads data bits 24-17 into the DBH register. It then writes bits 16-1 to the memory address encoding the A and F fields. Up to this point the sequence is the same as before. Now the 0715 responds to the VAX as if the SCI 2280 had responded while the SCI 2280 continues with the CAMAC operation. The VAX now reads a CSR in the 0715 check a status bit which signals completion of the CAMAC operation. It can then read the SCI 2280 CSR to get the Q and X responses. When a read operation is executed the 0715 returns dummy data in response to the memory read that initiated the action. The VAX must determine completion of the operation by reading the status bit in the 0715 CSR. The VAX must read data

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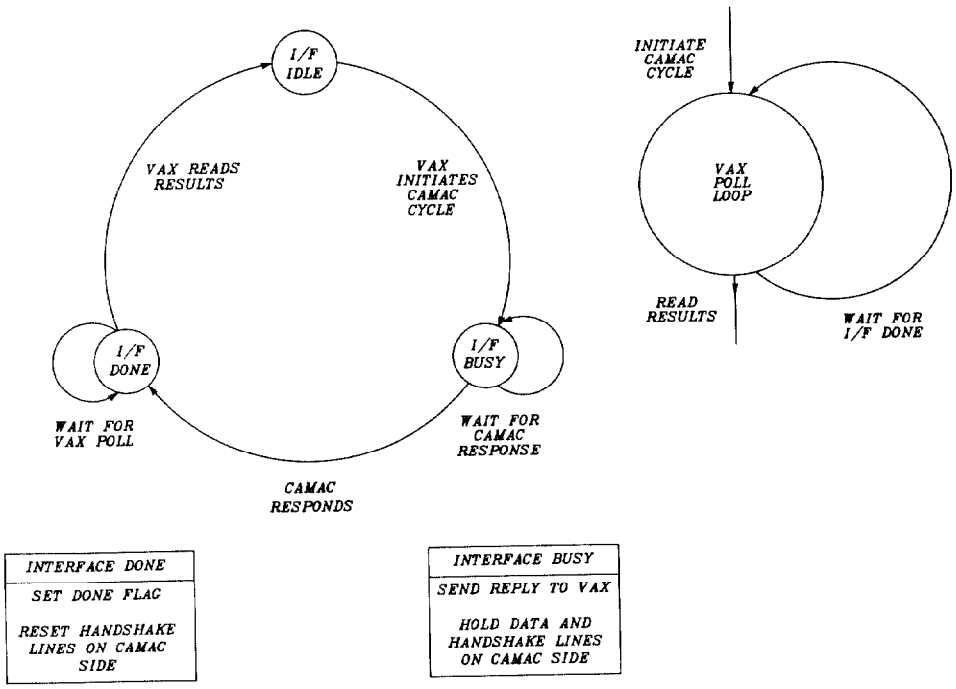

Figure 1: VAX timing is independent of CAMAC timing

bits 16-1 from a register in the 0715 and bits 24-17 from the DBH register in the SCI 2280. Q and X are saved in the SCI 2280 CSR as before.

TRIUMF 0715 Interface

With the TRIUMF 0715 interface in the system the VAX sees CAMAC operations complete within its timeout period and the SCI 2280 sees a Q-Bus with no limit on the duration of the control signals.

The 0715 has three 16-bit registers. The CSR register contains CAMAC operation BUSY and DONE status flags and interface ENABLE and TRANSPARENT mode and status bits. The DATA_WORD_LOW (DWL) and WRITE_DATA registers contains the low-order 16 bits for CAMAC data transfer operations. The interface powers-up with all functions disabled except for reading and writing the 0715 CSR register itself. The VAX sets the ENABLE bit to allow access to the SCI 2280. The TRANSPARENT mode bit controls the way the VAX accesses the SCI 2280 and CAMAC.

When the VAX sets the TRANSPARENT mode bit it can access CAMAC through the SCI 2280 in the same way as it does when the 0715 is not in the system. In this mode the only 0715 register visible to the VAX is the CSR. The sequence of operations for a CAMAC cycle is not modified and VAX timeouts can occur for long CAMAC cycles.

The 0715 Q-Bus latching functions are activated by clearing the TRANSPARENT mode bit. The 0715 DWL register becomes visible to the VAX and the BUSY and DONE status flags in the 0715 CSR have significance. CAMAC operations now follow the sequence described above. The 0715 BUSY flag is set when the initiating read or write memory cycle completes. The DONE flag is cleared and this combination of these two flags indicates a CAMAC operation is in progress but not completed. The handshaking signal from the SCI 2280 to the 0715 indicating the end of CAMAC operation causes the DONE flag to be set and the BUSY flag to be cleared. When the VAX reads this combination of BUSY and DONE in the 0715 CSR it knows that the CAMAC operation finished and data are available. Read operation data are saved in the 0715 DWL and SCI 2280 DBH registers. Write data are held in the 0715 WRITE_DATA register for the duration of CAMAC cycle. Q and X are saved in the SCI 2280 CSR for all operations.

Block Diagram

A block diagram of the interface is shown in Figure 3. The two data registers, WRITE_DATA and DWL, hold CAMAC operation data. WRITE_DATA holds data during CAMAC write operations and DWL contains the data returned from a CAMAC read operation.

The ADDRESS_DECODE block monitors the Q-Bus address lines and latches decoded addresses at the Q-Bus SYNC time. In the transparent mode the 0715 takes no action unless its CSR is addressed. In the non-transparent mode it enables its latch logic for valid CAMAC addresses. Valid addresses are those which match the addresses the associated SCI 2280 is configured to recognize. When the SCI 2280 is executing a CAMAC cycle addresses other than the 0715 CSR are disabled to prevent clashes with the ongoing operation.

The INTERFACE_CONTROL block generates signals to control the bus transceivers and controls Q-Bus timing to the SCI 2280. This block implements the wait state logic that allows extended timing for lengthy CAMAC cycles. The control signal latches make up the LATCHED_LOGIC block. Q-Bus handshaking with the VAX is handled by the QBUS_LOGIC block.

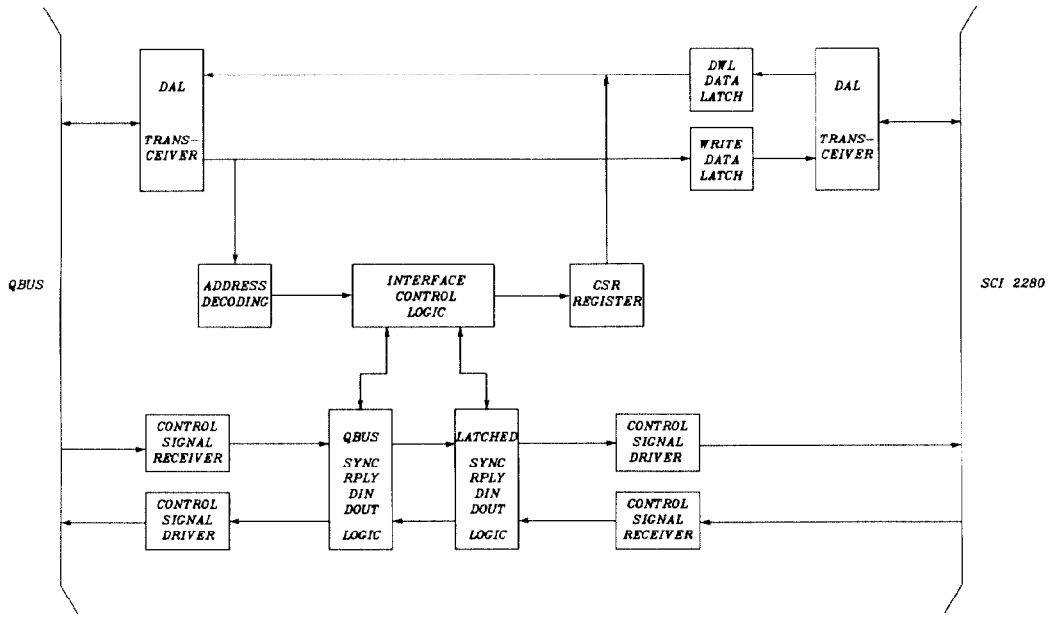

Figure 2: TRIUMF 0715 interface

Data paths through the module are a function of the decoded address and the 0715 operating mode. Addresses matching the SCI 2280 CSR and DBH registers allow data to be passed through unaltered, the module appears transparent to the SCI 2280 and to the VAX. Addresses which map into the CAMAC command space force data to be latched in the DWL and WRITE_DATA registers if the 0715 is in the non-transparent mode.

Test Results

The interface was bench tested with a VAX 3500 and simulated branch delay. No errors were detected with total delays greater than 25 μS. The maximum delay was limited by timeouts in the crate controller and SCI 2280 modules in the executive crate. These adjustable timeouts are set to a value which allows the longest anticipated CAMAC operation to run to completion but does time-out to prevent an indefinite delay due to failed operations.

A CAMAC cycle rate of approximately 12,000 operations/S was achieved with the 25 μS delay. This compares with the 13,000 operations/S achieved in a system without the 0715 and operating on a CAMAC branch with a 3 μS delay.

Summary

Decoupling of the VAX from the delays in the CAMAC branch has been achieved at the expense of polling the 0715 to determine completion of the CAMAC operation and of doing a second memory read, this time from the 0715, to get the low-order data from a CAMAC read operation. These extra VAX memory accesses do not significantly increase the total time for a CAMAC operation. Q-Bus based computers can now be used at the executive crate level to access long CAMAC branches.

Acknowledgements

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References

[1] DEC Microsystems Handbook,
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[2] SCI 2280 Q22 System Crate Interface User Manual,
Petit-Lancy:Creative Electronic Systems S.A.