LNLS CONTROL SYSTEM CONCEPTUAL DESIGN

J.G.R.S. Franco, S. Furquim, O. Monteiro,
A.R. Rodrigues * and C.R. Scorzato

LNLS, C.P. 6192, 13081 - Campinas - SP - Brazil

Abstract

The general architeture of the LNLS (Laboratório Nacional de Luz Síncrotron) accelerators control system is presented. The system is mostly based on 8-bit microprocessors and can be made compatible with the VME standard.

1. Introduction

The final goal of the LNLS (Laboratório Nacional de Luz Síncrotron) is to operate two storage rings (VUV and x-rays) for the production of synchrotron light. These two rings will be injected by a 100 MeV LINAC and a synchrotron booster up to 2 GeV [1].

A study of the control system for the LNLS accelerators showed that most of it can be done by 8-bit microprocessors at the equipment level. In order to reduce costs in the initial phase while maintaining the compatibility with 16 and 32-bit microprocessors in the future, the option was made in favor of the VME bus structure, with a specially designed local bus. Only few types of circuit boards are necessary for assembling the system at this level. The other two levels of the system use commercially available computers.

2. Structure

The Control System is divided in three levels

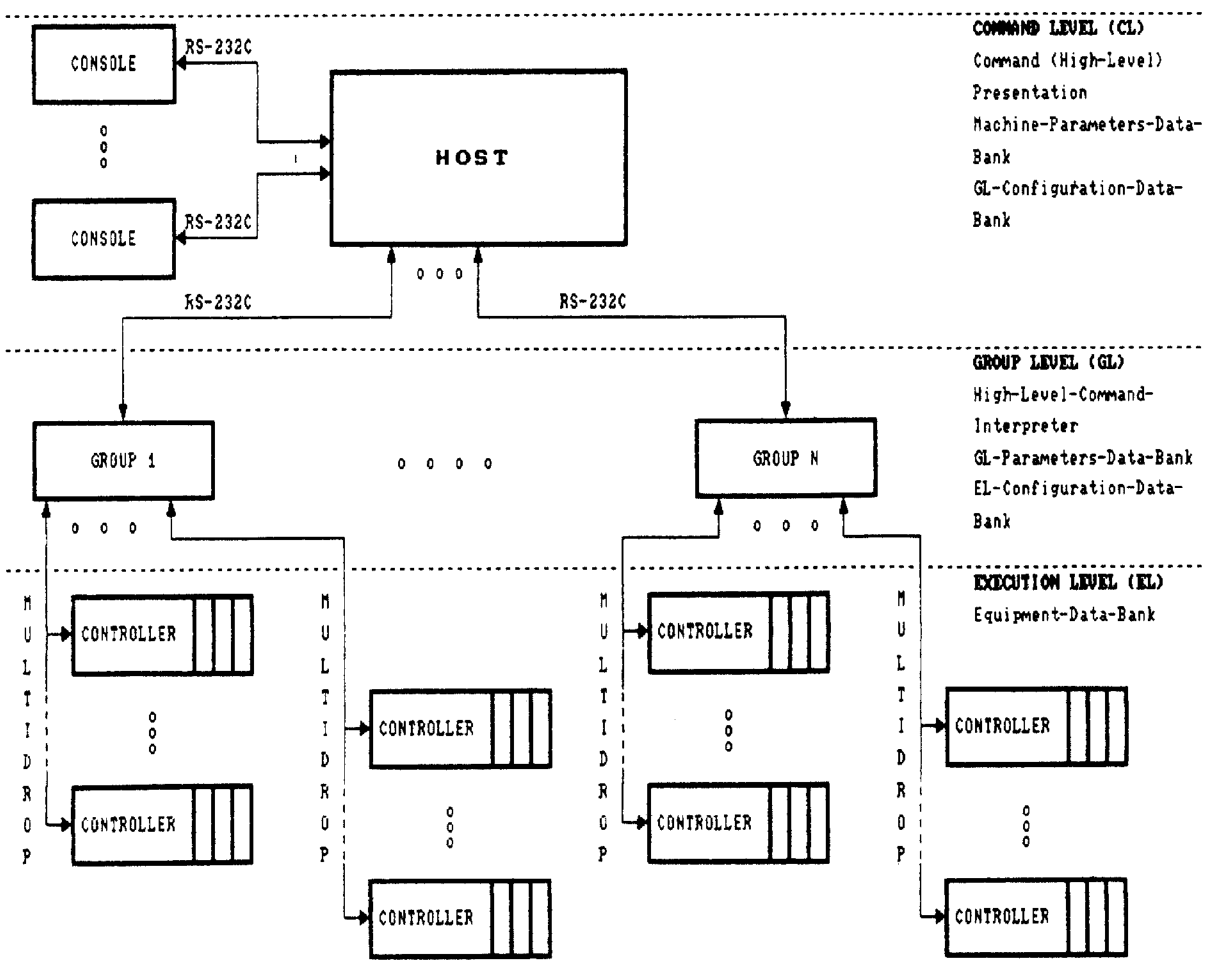

Figure 1 LNLS - Control System Structure

CH2669-0/89/0000-1651$01.00©1989 IEEE

PAC 1989

similarly to that proposed for the ESRF [2]: Command Level (CL), Group Level (GL) and Execution Level (EL; Figure 1). The Command Level provides the interface with the operators, keeps the machine parameters and GL configuration data banks and produces high level commands in response to the operators demands.

The accelerator complex is divided in sections at the Group Level. The Group Level links the Command Level and the Execution Level, interpreting the high level commands in order to optimize the communications in the system. Detailed data banks of group parameters and related Execution Level configuration are kept at this level.

The Execution Level, in direct contact with the equipment, performs the commands.

3. Computing Hardware

The Command Level employs the computer Cobra-1200 (Data General MV-4000), with 615 Mbytes of hard-disk, 4 Mbytes of RAM and a magnetic-tape drive. The operators use terminals and, when graphic information is needed, microcomputers (PC) or graphic terminals. They are also aided by touch screens, soft-knobs and mice.

In the Group Level there are VME crates (when the speed is important) and personal computers.

The Execution Level is formed by VME crates and local controllers (LOCO) under development in the LNLS as described below.

4. Communications Hardware

The exchange of data between the CL and the GL is in star configuration using the RS-232C standard in full-duplex and running at 38,400 baud.

The communication between GL and EL, uses multidrop serial lines RS-485, half-duplex and running at 19,200 baud. The default master computer is considered in GL. More than one multidrop can be defined for each GL computer (Figure 1).

The terminals and microcomputers for the operators use serial lines RS-232, running at 9,600 baud.

5. Messages

The communication in terms of software, between CL and GL is performed by High-Level-Messages (HLM): sequences of characters meaning commands and their parameters. These messages are simple, with a small number of arguments and directed to a specific microcomputer in the Group Level.

A High-Level-Message is interpreted at the Group Level, in terms of commands for each computer in the Execution Level. A HLM command can involve procedures in one or more controller in the EL.

Low-Level-Messages (LLM), between GL and EL are more complex than HLM. Each carries an address for the LOCO, adresses for modules, commands and data.

Is easy to see that the star distribution makes the messages less complex than the multi-drop. However, when working with many controllers, the hardware necessary in a star distribution may be unreasonably high.

6. Software and Data-banks

In the Command Level the software receives instructions from operators, checks the legality, transforms the command into messages, sends them to the GL and saves the modified parameters.

Periodically, the software verifies the status of equipments, the interlock system and display late information about the accelerators. All this information is kept in a Machine-Parameters-Data-Bank.

The Group Level configuration is also kept in a GL-Configuration-Data-Bank: a compact lay-out of the accelerator complex, to help in the interpretation of the operators instructions, presentation of information and to address the commands to the GL.

In the Group Level the software receives and decodes the message, checks the command and parameters in the GL-Parameters-Data-Bank and EL-Configuration-Data-Bank, creates a new message (Low-Level-Message, LLM) and sends it to the Execution Level. This means tree different tasks: (a) receiving the HLM from the Command Level, translating this message and sending a new one to the Execution Level; (b) receiving the LLM from the Execution Level,

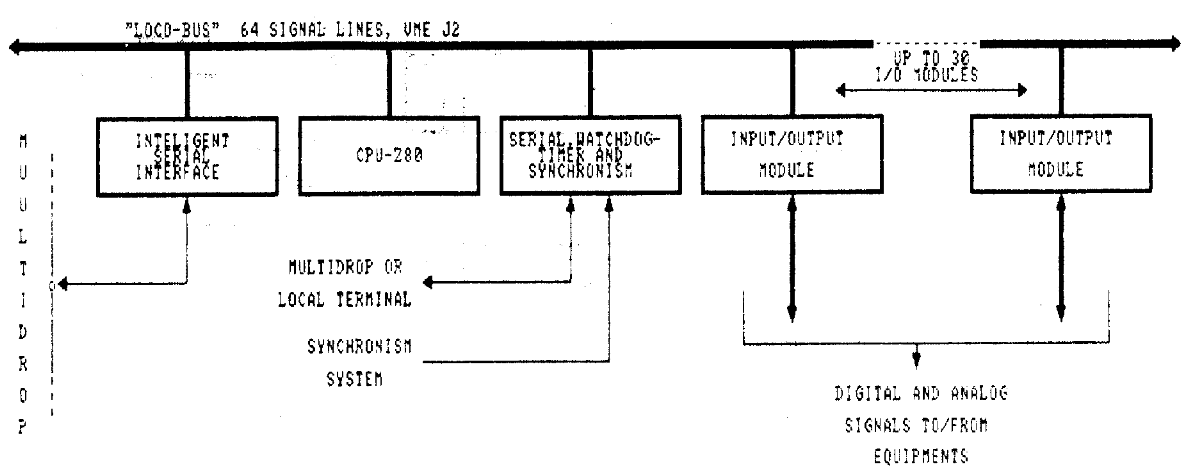

Figure 2 LOCO - Controller Architecture

translating and sending a new HLM to the Command Level and (c) updating the GL-Parameters-Data-Bank.

The software in the Execution Level will be a clear command interpreter. At the Execution Level there may be in some cases a Equipment-Data-Bank with information about the specific equipment under its control. This information is: equipment, logical name, target microcomputer, module address, commands and value. In most cases, the Equipment-Data-Bank is not essential, because the message received has all the necessary data. When the target microcomputer receives a message, it executes immediately the commands, modifying or reading the machine parameters. The Equipment-Data-Bank is necessary in special occasions described below.

7. Execution Level - Special Considerations

Sometimes the controllers in the Execution Level needs a periodical non-stop operation. This indicates that some of them cannot listen to the serial line all the time and in this case we need a two-processor controller and a Equipment Data-Bank. The additional processor is dedicated to the communication with the Group Level.

The EL uses two kinds of microcomputers: commercial VME crates and LOCO. The LOCO is a microcomputer in development at LNLS, based in Z-80 microprocessor, using the mechanical structure of VME, and the J2 unused signals backplane (Figure 2).

The LOCO-bus has 64 lines, most of them, similar to the Z-80. The others are: high-frequency clock, analog supply and 16 lines of decoded input/output-module select. Each of these lines are i/o-select of 16 sequential addresses, making the hardware of the decoder in the modules more clear and compact.

If in the future we need a powerful multiprocessor system (such as Experimental Stations), we can install LOCO microcomputers and I/O modules inside the VME crates, interfacing it, via a specially designed board, to commercial VME single board computers.

The LOCO microcomputer has a modular design, and uses few different types of circuit boards:
a)A module with a microprocessor Z-80, 8 Kbytes of EPROM, 4 Kbytes of RAM and a decoder of high input/output addresses (4 bits);
b)A module of input/output, with serial interface RS-485 (to connect to the multidrop or a local terminal) , watchdog timer, interval timer and input from the synchronism system;
c)A module of input/output, with interfaces to control the machine equipments. This module can be programed in hardware to perform several kinds of control signals such as: digital input/output, analog input/output and the combinations of these signals.
d)Intelligent serial interface, with a microprocessor Z-80, a serial interface, 2 Kbytes of RAM and 8 Kbytes of EPROM.

At this moment, the software and hardware in the Group and Execution Levels, are under development, with good results achieved so far in the single processor LOCO system.

References

[1] C.E.T. Gonçalves da Silva et al.,"LNLS: The Brazilian Synchrotron Light Laboratory", these proceedings.

[2] W.D. Klotz and C. Hervé, "The Conceptual Design of the ESRF Control System", ESRF-COMP-88-04, 1988.

*On leave from Instituto de Física e Química de São Carlos, Universidade de São Paulo, São Carlos, 13560 SP, Brasil.