BEAM POSITION MONITORS FOR THE CESR LINAC*

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ABSTRACT

A beam position monitor (BPM) system for the CESR linac has been developed that is capable of measuring 100 μm displacements for bunches with 10^8 particles. Each BPM consists of four stripline electrodes and associated fast analog and digital processing networks. Using 1 GHz bandwidth DMOS switching technology, a fast analog sampler has been implemented which captures the positive portion of a BPM stripline signal while rejecting the negative-going reflection. Reduced bandwidth post-sampling dual slope integration yields effective cancellation of analog switch charge injection and drift effects.

INTRODUCTION

The continuing quest for higher luminosity in CESR, the Cornell Electron Storage Ring, has resulted in the need for ever increasing average beam currents. This need can be fulfilled in part, in two ways. First, it can be achieved by decreasing the time between injection fills making the average current closer to the peak current. Second, it can be achieved by increasing the peak current. The success of both these strategies is mitigated by the subsequent increase in the "dead time" (the percentage of time when data cannot be taken) required for injection. A premium is thus placed on rapid injection. However, the increased linac currents needed for shorter injection times make the bunches in the linac more susceptible to position dependent transverse instabilities and it is these instabilities which now limit the current in the linac. In order to to overcome this problem an automated beam position monitoring (BPM) system has been designed for the linac.

BPM DESIGN

DESIGN REQUIREMENTS:

The design requirements were as follows:

i) Real time data acquisition (no averaging needed over multiple bunches)

ii) Resolution of 100 μm for bunches with 10^8 particles.

iii) Dedicated control computer so that the system can operate continuously without burdening the CESR control system.

iv) A dynamic range capable of operating with bunch numbers between 10^8 particles (the minimum positron bunch) and $2*10^{11}$ particles (the maximum electron bunch).

The system consists of 18 BPMs, of which 14 operate at any one time. Two BPMs are placed in the injector to the linac, one BPM is placed at the end of each of eight accelerating sections, and four BPMs are situated in both the electron and positron injection lines.

STRIPLINE ELECTRODES:

Each linac BPM consists of 4 stripline electrodes and associated electronics to measure and analyze the signals. Each stripline electrode is 60^o wide and has a characteristic impedance of 50 Ω. The wall current from the passing bunch will travel onto the electrodes creating a signal as shown in figure 1. The present linac stripline electrodes are approximately 40 cm in length with the upstream end coupled out of the pipe through a SMA vacuum feedthrough, and the downstream end shorted to ground. The signal produced by such a stripline electrode is bipolar in nature with a pair of pulses about 3 ns apart. Each pulse has half the total current on the electrode, or approximately 1/12 of the total beam current

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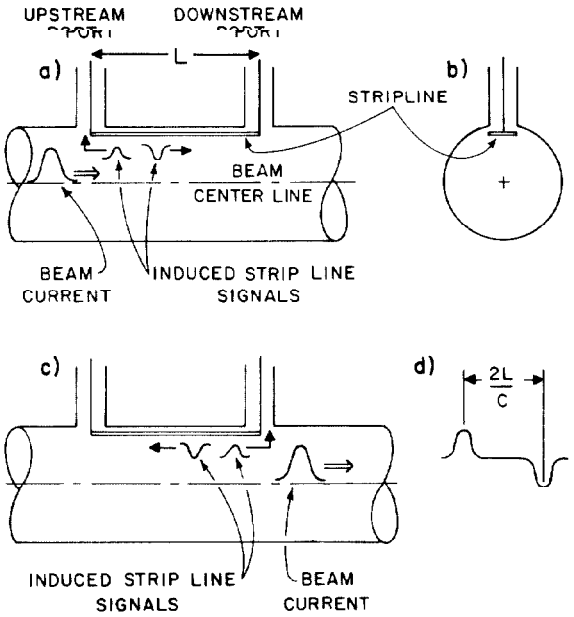

Figure 1. Stripline BPM: (a) shows a side view with the beam pulse arriving at the beginning of the stripline. (c) shows the situation just after the beam has passed the stripline. (d) shows the induced signal as observed on the upstream port.

The total wall current induced by a passing charge bunch will be divided among the 4 striplines according to the proximity of the beam to each stripline. Hence, the charge difference between two opposite electrodes will indicate the displacement of the bunch from the center of the pipe.

The subtraction of the stripline signals from opposite stripline electrodes is done with a 180 degree hybrid power splitter, immediately after the charge pulse is conducted out of the vacuum pipe. This is preferred to a subtraction later in the processing circuitry because then, any mismatch in component gains will result in an offset in the difference signal. The needed precision would require the matching of gains to better than one percent.

SAMPLE AND HOLD:

A block diagram of the BPM electronics is shown in figure 2 and a circuit diagram of the sample and hold circuit is shown in figure 3. Since the BPM signal is bipolar, a switch is required in order to do a measurement. The switch must be fast enough to admit the first pulse while rejecting the second. This requires a switch that can operate in one nanosecond. Since the subtraction of opposite electrodes has already been done, the first pulse of the difference signal can be either positive or negative. The switch, therefore, must be linear, and so a diode pulse stretcher is not suitable. However, there are several FET transistors available which have adequate speed and linearity and thus FET switches were used for the BPM system.

The FET requires a gate drive pulse which can effectively turn the device off in one nanosecond. The dynamic range of the sampler is limited at the high end by the amplitude of the drive pulse: As the signal pulse approaches the drive pulse in amplitude, it begins to affect the FET conductivity, hence producing nonlinearity or punch-through of unwanted signals. The drive pulse must also be as short as possible, since charge noise can only enter the sampling capacitor while the switch is on. The gate pulse is produced by a two stage direct-coupled FET amplifier with peaking coils. The output pulse is 15 ns long and 20 volts in amplitude, with a slew rate of 10 V/ns. The offset bias is -8 volts, and hence the pulse is at 12 volts. This results in linear response for

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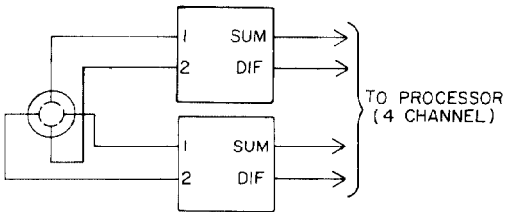
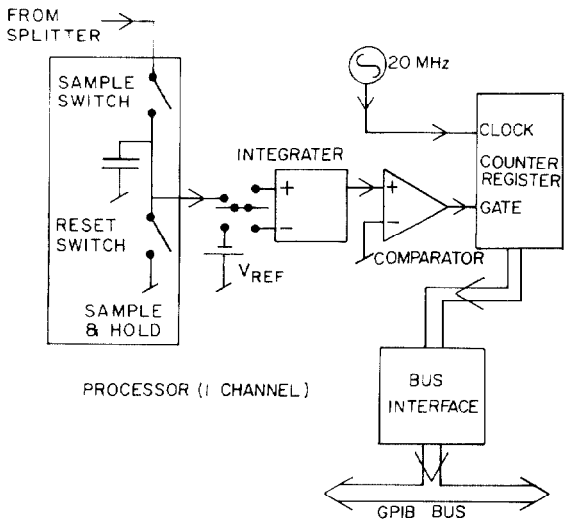
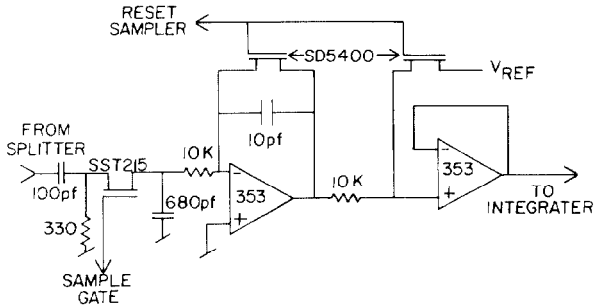


180° HYBRID
POWER SPLITTERS



BPM SYSTEM BLOCK DIAGRAM

Figure 2. Block diagram of the BPM electronics



DETAIL OF SAMPLE/HOLD & V_{REF}

Figure 3. Schematic diagram of the sample and hold circuit.

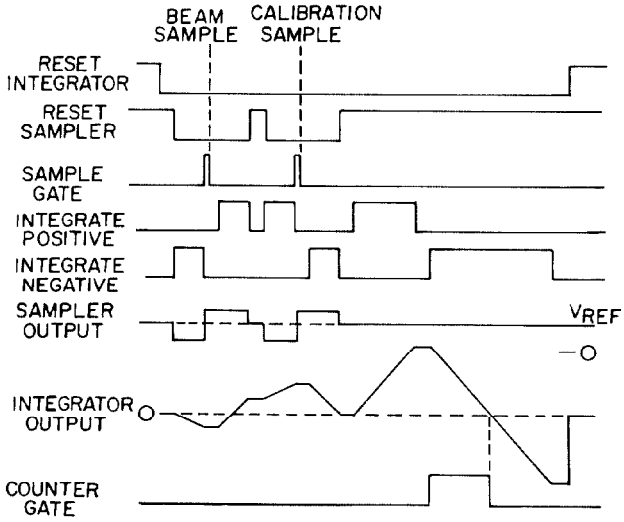
charge pulses of +/- 80 pC.

The sampler has a charge gain of 100 mV/pC. This is sufficient to make noise contributions from later processing stages unimportant. The internal noise is due to the input noise of the sampler amplifier. The measured RMS charge noise is 5 fC, making the dynamic range of the sampler +/- 16000.

ANALOG PROCESSING:

Operation of the sampling switch transfers an additional error charge to the sampling capacitor. This charge is capacitively coupled from the gate electrode, and it is stranded on the drain or source as the transistor turns off. This charge is in the range of 1 to 10 pC. In order to meet the sensitivity requirements, this charge must be subtracted off with an accuracy of 10 fC, or one part in 10^3. The actual injected charge varies by several picocoulombs among individual devices, and also depends on parameters of the circuit.

The injected charge is removed by subtracting two measurements: A beam measurement where actual wall current is gated into the capacitor, and a calibration measurement which is



BPM SYSTEM TIMING DIAGRAM

Figure 4. BPM system timing diagram.

identical except that it is done at a time when no beam is in the linac.

In actual practice a second switch is required to reset the sampling capacitor. There are thus two injected charges to be removed and this requires four addition/subtraction steps as shown in figure 4.

For simplicity, the arithmetic is done with a differential integrator. At each stage of the measurement, the sampler output is gated into the integrator for a fixed interval.

ANALOG TO DIGITAL CONVERSION:

The integrator, which is used for charge subtraction, also acts as part of the A to D conversion system. After the measurement cycle the charge on the integrator capacitor is proportional to the charge in the input pulse. During the conversion the integrator is ramped to zero at a fixed rate while a clock signal is gated into a counter.

Matching the dynamic range of the sampler requires 15 bits of data. For various practical timing restrictions only 14 bits are conveniently available. This loss in precision is avoided in the difference signal A to D conversion by reducing the full scale charge (reducing the dynamic range) from 80 pC to 40 pC

The gated pulse train is accumulated in a combined counter/register, consisting of two 74LS590 devices. The counter is clocked at 20 MHz, for a maximum interval of 800 μs.

DATA COLLECTION AND PROCESSING:

The data is collected from the 14 BPM processors through a modified GPIB bus. The bus segments between processors are up to 16 meters in length, and the total bus length is 120 meters. Since the physical length of the GPIB bus is longer than it was designed for and since the number of loads in the present system is larger then the maximum design number, the bus is restricted to a chain topology with a terminator at each end. All data and control lines except for NDAC and NRFD are terminated with 135 ohms to 2.5 volts. The NDAC and NRFD lines, since they carry wired-AND signals, must be under-terminated. They are each terminated with exactly one standard GPIB terminator. The rise times of these signals limit the data transmission rate to 30 bytes per millisecond. Each BPM processor issues 8 bytes of data plus 2 bytes of parity and status information, and so the entire bus can be read out in 5 ms.

The bus is operated by an MVME133 microcomputer, which consists of a 68020 microprocessor, a 68881 floating point co-processor, and 1 Mbyte of memory. The computer is VME compatible, and operates the data collection bus through a commercial GPIB controller. The GPIB interface at the BPM processor is implemented with three 22V10 PAL devices.

Data is collected at the linac repetition rate of 60 Hz. The linac trigger is used to interrupt the MVME133 at maximum priority, which then collects data and updates statistical quantities such as running averages, standard deviations, and correlations. The CESR control system may issue an interrupt at lower priority, whereupon the MVME133 will transmit recent data and statistical summaries to the control system for display or trajectory correction. All other processing, such as data scaling and formating, is done between interrupts.

PACKAGING AND NOISE PROTECTION:

The sensitivity of the charge sampler requires protection from external noise produced by thyratron and SCR operation. Noise may be introduced through the power supply voltages, by ground loop coupling into the pulse input, or coupled directly into the analog circuitry.

To prevent the last possibility, the processor is placed in a completely shielded enclosure. The analog circuitry is miniaturized in the form of thick-film hybrids with surface-mount integrated circuits. As a result, the entire four processor channels, complete with bus interface, can be enclosed in a commercial 6" x 4" x 2 1/2" extruded aluminum box.

The extruded box is divided into two chambers: The "quiet" chamber contains the analog processors and gate drivers. It is entered only by the coaxial pulse inputs, gate signals, and power leads. The "noisy" chamber contains the bus interface and the sequencer which controls the analog processor.

The power leads are brought into the "noisy" chamber through RFI filters, and are filtered again as they are brought through to the "quiet" chamber. Inside the "quiet" chamber, the voltages are regulated down to eliminate any 60 Hz ripple.

Noise from 60 Hz ground loops is eliminated by the high-pass filter before the sampling switch. There remains the threat of RF ground loops penetrating the shield of the pulse cables. Semi-rigid cabling was considered, but ruled out due to a combination of radiation resistance problems and cost. Double shielded cable of the RG-55 type has been used, and no noise penetration has been observed in preliminary tests.

PERFORMANCE

A prototype BPM and Processor has been tested with both electron and positron beams, and the installed final version has been tested with electrons only. These tests verify the basic operation of the system and the noise performance. The RMS noise was observed to be 5 fC, the same as in bench tests.

The position sensitivity is defined as Qdiff/Qsum per unit displacement. The position sensitivity for a BPM with a stripline inner diameter of 3.5 cm is measured as 0.008/100 μm. Assuming that one twelfth of the total wall current appears in each electrode pulse, this translates to a minimum threshold of 3×10^7 particles to resolve position to 100 μm. The upper limit on sampler charge translates to an upper limit of 3×10^9 particles, or an effective dynamic range of 100 for a 100μm position measurement. Attenuators of 20 or 40 dB must thus precede the sampler for measurement of large electron beams.

ACKNOWLEDGMENTS

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