ACTIVE INTERLOCK FOR STORAGE RING INSERTION DEVICES*

J.L. Rothman and R.J. Nawrocky
National Synchrotron Light Source
Brookhaven National Laboratory
Upton, New York 11973

ABSTRACT

The insertion devices in the NSLS x-ray ring produce such intense photon beams that passive measures alone are not adequate to protect the vacuum chamber. An active interlock is used to prevent thermal damage from improperly steered electron beams. The interlock system measures the position of the electron beam on both sides of the insertion devices using pick-up electrodes and interrupts the RF if the beam moves outside a safe window. The interlock features redundant circuitry as well as an automatic testing procedure.

INTRODUCTION

Three new high power insertion devices are now coming on line in the NSLS x-ray ring. There will be two hybrid wigglers and one superconducting wiggler providing light to beam ports x-21, x-25, and x-17 respectively. Electron beams passing through the insertion devices at vertical angles greater than 1.6 mrad expose unprotected regions of the beampipe to intense X-rays. Since space constraints prevent adequate cooling of these areas with water, an active interlock is required to protect the chamber. An interlock based on beam position measurements makes use of detectors that already exist, requires minimal modifications to the ring, and responds faster than a system based on thermal measurements. Such a system can also be tested by generating a closed orbit distortion with trim magnets and monitoring the interlocks response.

SYSTEM DESIGN

Figure #1 is a block diagram of the interlock. A set of four PUEs are positioned on each side of an insertion device. The signal from each button is split and fed into two separate detectors for redundancy. The detectors provide X and Y output signals that are proportional to the displacement of the electron beam from the center of the beampipe. If the detector output exceeds safe limits the interlock logic opens one of the central relays, thereby interrupting the RF.

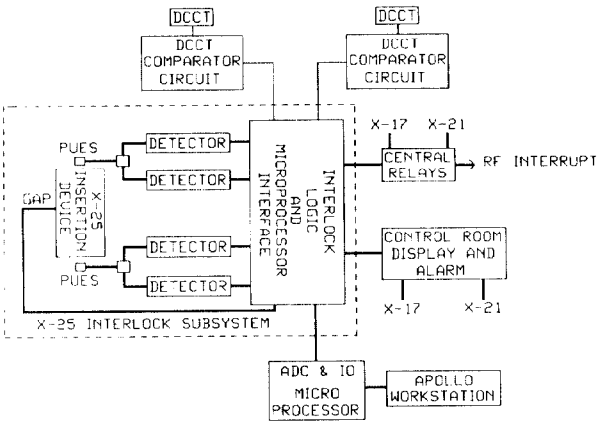

Figure 1. Interlock block diagram.

Logic status bits are then latched and provided to the workstation via the microprocessor and to the control room display. The interlock is disabled if the primary and backup gap bits show that the insertion device gap is open or if the outputs of both DCCT comparator circuits indicate that the beam current is below 3.75 mA. Where possible, control signals are designed to trip the RF when they are low. This insures that power failures will trip the RF rather than leave the machine unprotected.

INTERLOCK LOGIC AND MICROPROCESSOR INTERFACE

Figure #2 is a block diagram of the interlock logic and microprocessor interface. Each detector output is fed into a logic unit. The logic units receive gap status information from the microprocessor interface and beam current information directly from the DCCT comparator circuits. Logic status bits are latched in the interface unit and provided to the IO section of the microprocessor for use in the testing procedure.

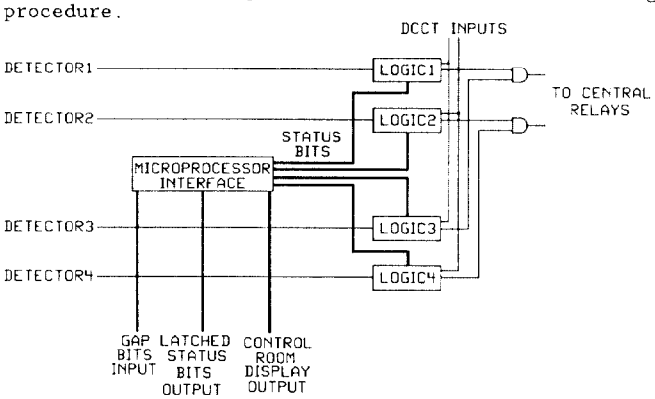

Figure 2. Interlock logic & microprocessor interface.

A functional diagram of the interlock logic is shown in Figure # 3. The X, Y and DCCT signals are buffered and sent to an ADC board in the micro. These signals will be used for calibration measurements and machine diagnostics. The Y and DCCT comparator signals are fed into window comparator circuits; if either of these signals deviates from the specified range of voltages the output of the window circuits will drop to zero.

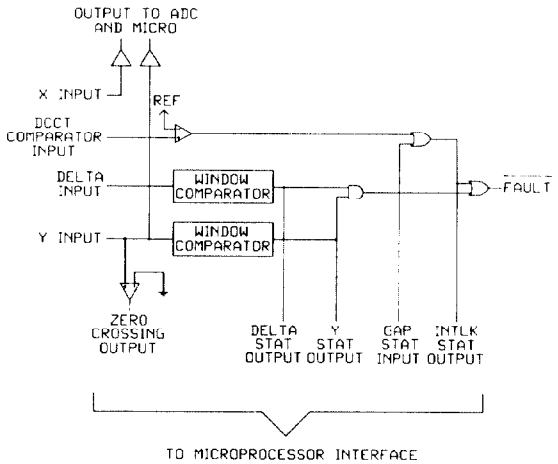

Figure 3. Interlock logic.

*This work was performed under the auspices of the U.S. Department of Energy.

CH2669-0/89/0000-0266$01.00©1989 IEEE

This logical 0 propagates through the logic and results in an opened relay. Loss of current in the relay interrupts the RF. The X axis displacement signal is not used to interrupt the RF since the insertion devices are passively safe for horizontally missteered beams. If the beam current is below 3.75 mA the DCCT comparator signal will be 15V. This forces the output of the OR gates to a logical 1 and prevents the fault signal from interrupting the RF. If either of the DCCT signals are OV and either the Y or delta signals are out of range the interlock interrupts the RF and dumps the beam. This causes the DCCT comparator signals to return to 15V and in turn restore the RF. The OR gates can also be forced high by the gap status bit being high. A one on the gap status bit indicates that the insertion device gap is open. The zero crossing, y status, delta status, and interlock status bits are sent to the microprocessor interface. These signals are then sent to the micro and used for the testing procedure. Four logic circuits are located in each subsystem; a primary and backup for the upstream PUEs and a primary and backup for the downstream PUEs.

As shown in Figure 4, the microprocessor interface contains a first event latch that latches the input when any of the Y status or delta status bits go low. This insures that information is not lost when the beam dumps. The interlock status bits are monitored by a four input AND gate and a four input NOR gate. If the output of the AND gate goes high it indicates that all four sets of interlock logic in a given subsystem are disabled. If the output of the NOR gate is high all four sets of logic are enabled. The latch can be reset or inhibited by drawing the reset line high. This can be done manually from the control room or automatically by the micro. The latch status bit goes high whenever the circuit is latched. This bit is monitored in the control room and by the local micro. The gap signals are received from the insertion devices, split and sent to the logic units.

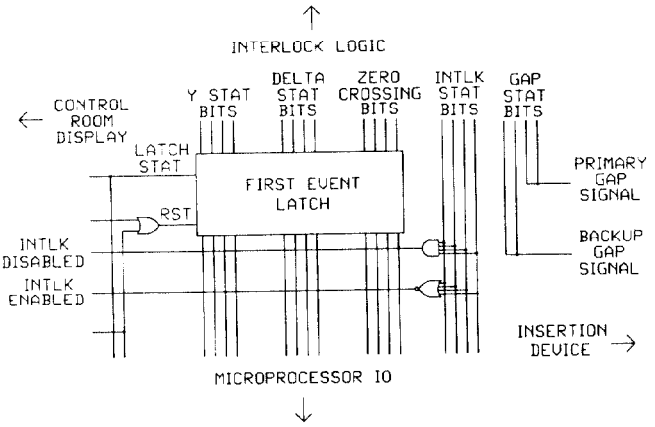

Figure 4. Microprocessor interface.

TESTING PROCEDURE

Prior to each fill the operator injects 2.5mA into the ring and runs the testing program on the workstation. The program inhibits the first event latches. It then generates large angle closed orbit distortions in the straight sections of each of the insertion devices one after the other and monitors the status bits generated by each subsystem. At low currents the interlock status bits will all be high. Generating a large downward angle distortion causes all of the Y status bits to go low. The upstream zero crossing bits will be high and the downstream zero crossing bits will be low. Generating an upward angle distortion also sets all the Y status bits low but reverses the state of the zero crossing bits.

After completing this portion of the test the operator injects more current into the ring, bringing the total current up to 5mA. This enables the interlock and the interlock status bits will all be low. The program then proceeds to generate another closed orbit distortion in one of the insertion device straight sections and the 5 mA will be dumped by the interlock. If the interlock passes the test the operator can proceed with normal injection.

ACKNOWLEDGEMENTS

We would like to thank Jack Tallent for outstanding technical support.

REFERENCES

[1] R. Biscardi, J.W. Bittner, "Switched Detector for Beam Position Monitor," this conference.