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### **RF PULSE COMPRESSION EXPERIMENT AT SLAC\***

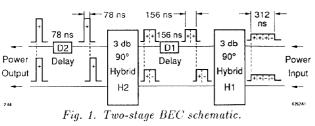
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### ABSTRACT

Using RF pulse compression it will be possible to boost a 50-100 MW output, expected from high power microwave tubes operating in the 10-20 GHz frequency range, to the 300-600 MW level required by the next generation of high gradient linear colliders. Experiments have been performed at Stanford Linear Accelerator Center to test, at low power, a two-stage binary energy compressor (BEC)<sup>1</sup> operating at 11.424 GHz. Using over-moded delay lines and 3 dB hybrid couplers, a 312 ns pulse was compressed to 78 ns, giving a power multiplication ratio of  $\sim 3.2$ , and a power efficiency of 81%. Individual component insertion losses were measured to be in the range of 0.6% to 8.5%. Overall efficiency calculated using these values agreed with measured values to  $\sim 1.4\%$ . Using best values of the measured component insertion losses, the efficiency of a proposed high power test of a three-stage BEC is estimated to be 71%, with a power multiplication of  $\sim 5.7$ .

#### 1. EXPERIMENTAL APPARATUS

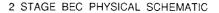
The principle of operation of a BEC is described in detail elsewhere.<sup>1,2</sup> Figure 1 shows a schematic of a two-stage BEC. Briefly, it works as follows: the two RF inputs to the BEC are phase-coded into time bins with 0° and 180° phases, denoted by (+) and (-), respectively. Hybrid H1 combines the pulse trains to produce two outputs, each at twice the power and half the duration, properly coded for the next stage, with the time relationships shown. Delay line D1 (156 ns) serves to align the two pulse trains so that they are coincident in time at the input to hybrid H2, which again doubles the peak power and halves the time duration. Delay line D2 (78 ns) serves to align the final two pulse trains so they are coincident in time at the acceleration sections of a linac. 2 STAGE BEC SCHEMATIC

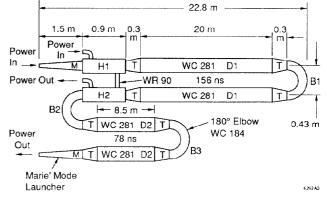


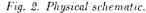
For reasonable efficiencies, the delay line and hybrid losses have to be of the order of tenths of dB. Therefore, overmoded 2.81-in.-diameter circular waveguide (WC 281) was chosen for the delay lines, and standard rectangular WR 90 X-band waveguide was used for the non-delayed connections. The 3 dB hybrids had one circular 1.84-in.-diameter (WC 184) port and one WR 90 port each. All delay line bends were fabricated from corrugated 1.84-in.-diameter circular waveguide. Typical attenuations of these guides are given in Table I.

Waveguide	Size (inch)	$\mathrm{dB}/\mu\mathrm{s}$	dB/m
WC 281	2.81 diam.	1.1	0.004
WC 184	1.84 diam.	3.6	0.0066
WR 90	$0.9 \times 0.4$	19	0.078

 Work supported by the Department of Energy, contract DE-AC03-76SF00515. Marié-type mode launchers were used to convert from the  $TE_{10}$  mode in rectangular guide to the circular  $TE_{01}$  mode in circular guide. A schematic of the mechanical arrangement is shown in Fig. 2. The cosine curve tapers (T) shown were used as transitions between WC 281 and WC 184 wave guides. An electrical schematic of the same apparatus with series connected Phase Shift Keyers (PSK's) is shown in Fig. 3. All RF power at the directional couplers was measured with tunnel diode detectors and a fast oscilloscope. The RF was phase modulated with 0° to 180° PSK's driven by a TTL modulation generator.







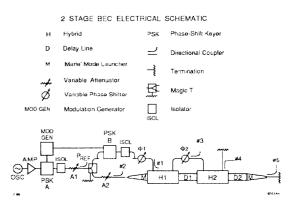
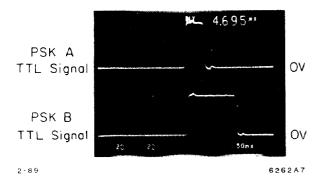


Fig. 3. Two-stage BEC electrical schematic.

# 2. PROCEDURE AND RESULTS

With no phase modulation applied, attenuator A2 and phase shifter  $\phi 1$  in Fig. 3 were adjusted to give minimum power at directional coupler #3. Modulation was then applied with TTL signals to PSK A and PSK B (Fig. 4). Phase shifter  $\phi 2$  was adjusted to maximize the peak output power and minimize the background power at directional couplers #4 and #5 (Fig. 5). Since RF power was not gated, Fig. 5 shows C.W. unmodulated power present outside of the 312-ns-long phase-modulated pulse train window. The unmodulated power level was 6 dB below the peak power in the output pulse, as expected.



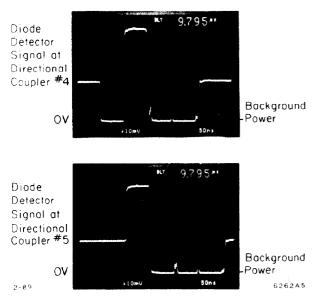


Fig. 4. TTL drive signals for PSK's.

Fig. 5. Diode detector waveforms at BEC outputs.

Input and output power measurements were made as follows. A diode detector was connected to directional coupler #1, and its voltage measured on an oscilloscope. A power meter connected at  $P_{REF}$  was set to 0 dB. The diode detector was then moved to directional couplers #2, #4, and #5. At each location, variable attenuator A1 was adjusted to give the same diode detector voltage as at coupler #1 and the  $P_{REF}$  relative power reading was noted. Thus all power measurements were made relative to one power input to the BEC. The relative power readings were then corrected for the individual directional coupler's coupling factor. Table II summarizes the results of five typical measurements.

Table 1	Ι
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RELATIVE POWER AT DIRECTIONAL COUPLER (dB)				EFFICIENCY (%)	POWER MULTIPLICATION FACTOR
#1	#2	#4	#5		
0, -0.48	0.30	5.24	5.02	80.7	3.23
0, -0.51	0.07	5.14	4.90	81.1	3.24
0, -0.47	0.11	5.17	4.92	81.0	3.24
0, -0.47	0.12	5.19	4.95	81.3	3.25
0, -0.48	0.12	5.17	4.92	80.9	3.24

More than one power reading appears in the #1 column because PSK B had different insertion losses depending on its modulation state, as shown in Fig. 6. Here the first and third power transients are due to PSK B changing state, and the second transient is due to PSK A changing state. The different PSK insertion losses were taken into account in calculating the overall power efficiency of ~81%.

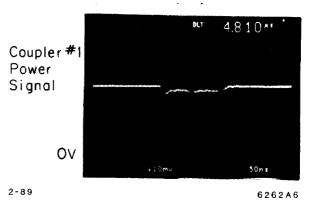


Fig. 6. Diode detector waveforms at directional coupler #1 showing PSK insertion loss changes and power transients.

# 3. COMPONENT INSERTION LOSSES AND CALCULATED BEC PERFORMANCE

Insertion losses of all components were measured, except for the delay line losses, which were calculated. Table III summarizes the results. Hybrid insertion losses differed depending on whether power was combined into the circular or rectangular ports and were not the same for both hybrids, indicating that better design could lower these losses. Differences in the losses of 180° bends B1, B2, and B3 were attributed to mode conversion, again indicating that proper design could decrease them.

Table III

Devic	Insertion Loss (%)	
Hybrid	H1 (circular)	1
	H1 (rectangular)	3
	H2 (circular)	3
	H2 (rectangular)	4.5
Taper	Т	0.2
Delay	D1 (40 m)	3.7
	D2 (17 m)	1.6
180° Bend	<b>B</b> 1	2.1
	B2	1.6
	B3	2.5
Marié Mode Launcher	М	4.7
WR 90 Guide		$5.9 \rightarrow 8.5$

Since the ambient temperature varied by up to 20°F, phase shifter  $\phi 2$  had to be re-adjusted often during the BEC tests to compensate for phase shifts caused by delay line length changes. This is the reason for the range of insertion loss for the WR 90 non-delayed connection in Table III. In any high power device this phase-shifting would be done in the circular guide, where a practically lossless phase shifter design is possible because of the  $TE_{01}$  mode's azimuthal current flow. Table IV summarizes power loss distributions in the BEC. It is seen that the total power efficiency of the two-stage BEC is about 80%.

Table IV

BEC POWER LOSS DISTRIBUTION FOR EQUAL			
AMPLITUDE INPUTS			
Device	Power Loss (%)		
Marié Launchers	4.7		
Hybrids H1 & H2	5.6		
WC 184 $\rightarrow$ WC 281 Tapers	0.6		
180° Bends	3.1		
WR 90 Guide	$2.95 \rightarrow 4.25$		
Delay Line D1	1.85		
D2	0.8		
	Total 19.6 $\rightarrow$ 20.90		

Using the measured component losses, the peak power outputs for the BEC were calculated and are compared to five typical measured values in Table V.

In all cases, measured total power output agrees well with the calculated power, being at most  $\sim 1.4\%$  lower. This is within the range of the phase shifter  $\phi 2$  insertion loss uncertainty due to its variable setting.

Table V

Output Power at Directional Coupler (Arb. Units)					
#4 #5					
Meas.	Calc.	Meas.	Calc.		
3.34	$3.46 \rightarrow 3.41$	3.18	$3.15 \rightarrow 3.10$		
3.27	$3.36 \rightarrow 3.31$	3.09	$3.06 \rightarrow 3.02$		
3.29	$3.38 \rightarrow 3.34$	3.11	$3.08 \rightarrow 3.04$		
3.30	$3.38 \rightarrow 3.34$	3.13	$3.08 \rightarrow 3.04$		
3.29	$3.38 \rightarrow 3.34$	3.11	$3.08 \rightarrow 3.04$		

# 3. ESTIMATE OF THREE-STAGE, ONE KLYSTRON BEC EFFICIENCY

A three-stage high power test of a BEC is in the design stage at Stanford Linear Accelerator Center (SLAC). As proposed by Latham<sup>3</sup>, it will be driven by a single 100 MW klystron being developed at SLAC.<sup>4</sup> A 770-ns-long RF pulse will be compressed to 70 ns. Figure 7 shows this BEC schematically; the symbols have the same meaning as in Fig. 2. Notice that the two outputs of the three-stage BEC are again combined in hybrid H4 to obtain a single higher power pulse for high gradient accelerator structure tests. Using the lower component insertion losses measured in the two-stage BEC experiment the efficiency of such a three-stage BEC is calculated to be 71%, with a power multiplication factor of ~ 5.7. If the klystron produces 100 MW, the single source three-stage BEC would produce a peak power of 285 MW, and if the outputs are combined the pulse peak power should be 567 MW. A 1-m-long accelerator section<sup>5</sup> with  $\beta_g = 0.48, \eta_s = 0.71, s = 911\Omega/ps - m$  powered by this combined output pulse would yield a gradient of 160 MV/m, about eight times the SLC gradient and 1.7 times greater than that required for the SLAC ILC linear collider design.<sup>6</sup>

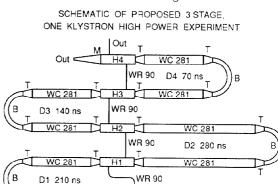


Fig. 7. Schematic of proposed three-stage, one klystron high power experiment.

2 Output Klystron

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# 4. HIGH POWER OPERATION OF BEC

Although not demonstrated, we believe that the two-stage BEC is high power capable. Peak surface fields in the hybrid slots and in the WR 90 waveguide at 567 MW output power are estimated at  $\sim 80$  MV/m, a factor of 5.6 times lower than the 450 MV/m peak surface fields in the accelerator section described above. These fields are well below those obtained in practice.<sup>7</sup> The three-stage vacuum-tight BEC system, scheduled for completion in September of this year, will be tested under various vacuum cleanliness conditions. Large cost savings can be realized if the cleanliness requirements can be relaxed.

#### 5. SUMMARY

High efficiency operation (~81%) of a two-stage BEC operating at 11.4 GHz has been demonstrated at low power with components that are estimated to be high power capable. Component insertion loss values indicate that further gains in efficiency are possible with better design. Estimates show that a proposed three-stage high power BEC at SLAC should produce peak power levels of ~ 567 MW for testing high gradient accelerator structures at gradients up to 160 MV/m.

# REFERENCES

- Z. D. Farkas, Binary Peak Power Multiplier and its Application to Linear Accelerator Design, IEEE Tran. MIT-34, p. 1036, October 1986.
- Z. D. Farkas et al., RF Pulse Compression Development, SLAC/AP-59, AAS Note-28, October 1987.
- P. E. Latham, The Use of a Single Source to Drive a Binary Peak Power Multiplier, 1988 Linear Accelerator Conference, Williamsburg, VA, October 3-7, 1988.
- 4. K. Eppley, Design of a 100 MW X-Band Klystron, this conference.
- 5. Z. D. Farkas, The Roles of Frequency and Aperture in Linear Accelerator Design, 1988 Linear Accelerator Conference, Williamsburg, VA, October 3-7, 1988.
- 6. R. B. Palmer, SLAC/AAS-Note 39, (November 1988).
- G. A. Loew et al., RF Breakdown in Room Temperature Electron Linac Structures, XIII International Symposium on Discharges and Electrical Insulation in Vacuum, Paris, France, June 27-30, 1988.