# HIGH PRECISION POWER SUPPLIES FOR THE NATIONAL SYNCHROTRON LIGHT SOURCE

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## Summary

The Phase II construction project requires the replacement of the X-ray ring main magnet power supplies with new units capable of achieving 3 GeV operation, and providing better regulation than the existing units.

## Introduction

In the operation of the Light Source, there is a constant drive to upgrade performance, in this instance, the energy and beam position. Since operation was started, the tolerance for beam position has been tightened considerably, and with the installation of the insertion devices is expected to increase by an order of magnitude.

Since beam stability depends to a considerable degree on the stability of the magnet power supplies, and for Phase II it is desired to push for 3 GeV operation, it was required that new power supplies be obtained for the quadrupoles and sextupoles. These power supplies were to have the lowest ripple that could be reasonably achieved, and were to have a current regulation of better than 10 PPM. In addition, since they operate over a 5:1 voltage range, it was considered desirable to ensure that they operated with a good power factor over the operating range. The dipole power supply was modified to use the techniques employed in the smaller supplies.

## Bridge Rectifier

A schematic of the power supply is shown in Fig. 1. The bridge configuration chosen was that of Stefanovic.[1] This provided several advantages, namely, lower harmonic content on the dc side, lower requirement for reactive power, especially at reduced dc voltages, lower rms line current at reduced power output, and compatability with the existing control system. Since inversion is not required, thyristors 7,8 are replaced by diodes.

An input auto-transformer, not shown, allows the peak output voltage to be set over a 2:1 range in six steps to allow matching the power supply to the load for optimum power factor at full energy. This is followed by two delta-star transformers which give the ± 15° phase shift required for 12 pulse operation, and to prevent triple harmonics from entering the ac system. The two bridges are paralleled by an interphase transformer. The chokes are wound such that the leakage capacitance to ground is symmetrical, and the power transformers are provided with a shield between the primary and secondary. Two stages of filtering are provided. The first is a passive LC filter comprised of L1, C1, C2, and R1. The second is an active filter comprised of L2 and Q1.

## Control System

The control system used has been previously described,[2] with the following improvements.

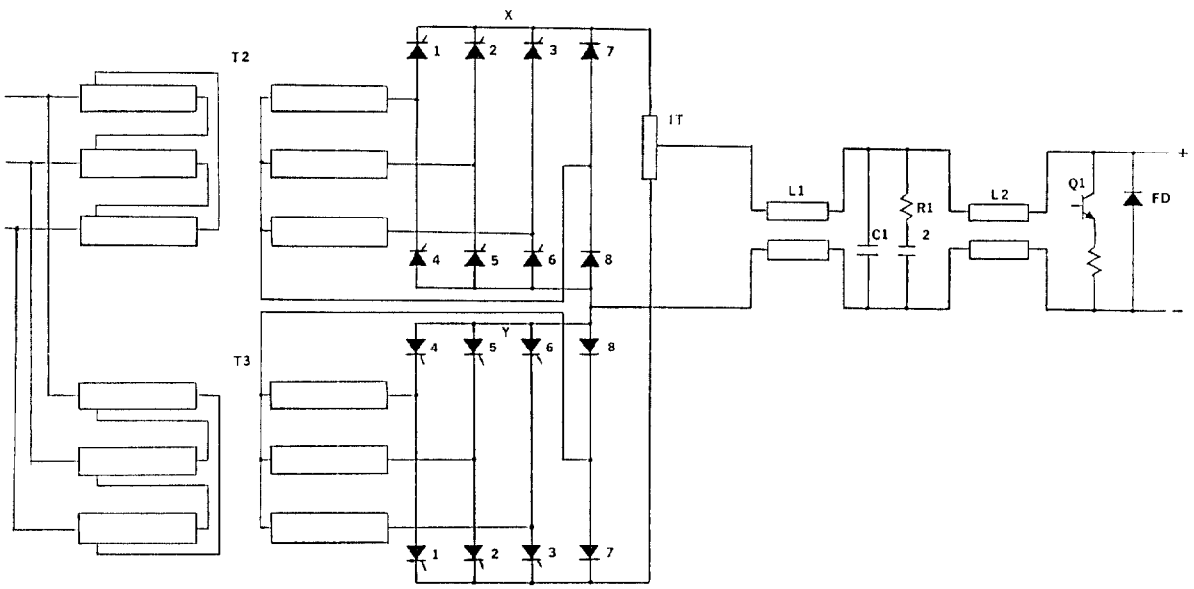


Figure 1

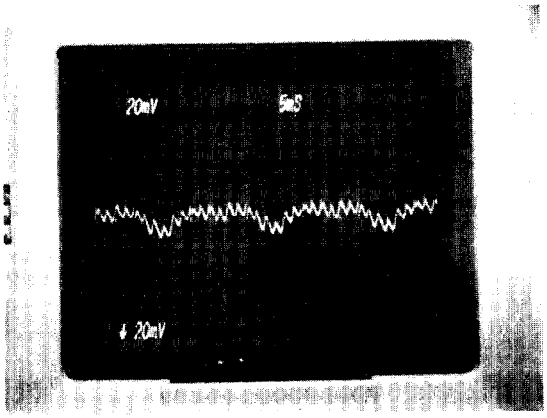


Figure 2 Sub-Harmonic Reduction OFF
Output 100 Volts, 120 amps,
2V/cm. AC Coupled.

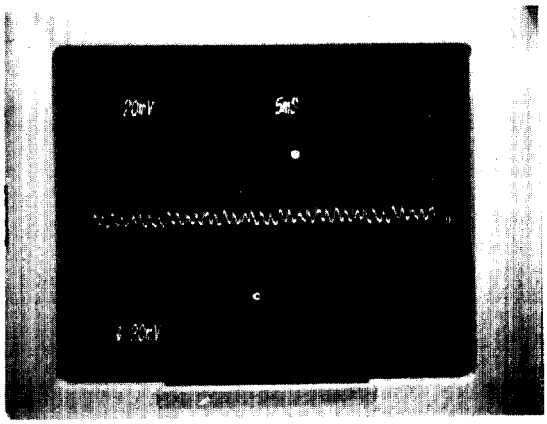


Figure 3 Sub-Harmonic Reduction ON
Output 100 Volts, 120 amps,
2V/cm, AC Coupled.

Phase Locked Loop

The original hard-wired PLL has been replaced with a micro-processor based device. This has allowed better fault monitoring and has reduced jitter to <5$\mu$s.

Sub-Harmonic Ripple Correction

Ripple correction is obtained with a custom designed controller board using a 8085 micro processor and a Am9511A coprocessor. The control program is written in assembly language utilizing a stripped down version of the standard NSLS control monitor and application specific subroutines. Twelve phase samples are obtained from an input voltage integrator which integrates over a 30 degree range (± 15 degrees from the SCR trigger point) via an A/D converter. The sampling routine is interrupt driven. This interrupt level is disabled at the completion of a full sample to allow the calculation phase to proceed. Various tests are performed on the input such as A/D saturation limits, correct sequencing of phases, etc. and the average dc voltage is calculated. This average dc value is adjusted for overall system gain, filtered and sent to a DAC to null out the dc component. As this component is reduced, front end gain is increased for higher ripple resolution. The overall software loop gain factor is maintained at a constant value of 256 to simplify correction calculations. A Fourier transform is performed on the twelve input phases for six harmonics (60 HZ through 360 Hz) followed by an inverse transform. Sine/cosine values are rapidly obtained via a phase/harmonic offset into a stored table. Each harmonic is assigned a weighting factor and enabling bit allowing full selection of which harmonics are processed. The final correction factors are digitally filtered, limit tested, and scaled for gain factor and output counter conversion. They are then transmitted to a dual output buffer where one section is controlling while the other is available for loading the next set of corrections. Following buffer loading and control a scheduling algorithm is executed, prior to enabling the input interrupt level, which periodically switches the input multiplexor to a five volt reference and ground before starting the next phase sample cycle. Input phase voltages are corrected for any detected ground offset. Present clock rates produce two to three correction cycles per second and the existing hardware is capable of running twice as fast if required. Fig. 2 and 3 show a quadrupole supply with the sub-harmonic ripple correction switched off in Fig. 2 and on in Fig. 3.

Active Filter

The active filter serves to attenuate the 720Hz ripple which is not suppressed by the LC filter and is based on the work of Cilyo et al.[3] The essential difference is that voltage feedback by means of a digital filter is used, and biasing of the power transistor is dynamic and is programmed by a control circuit for optimum dynamic range.

References

1. V. R. Stefanovic, "Power Factor Improvement with a Modified Phase-Controlled Converter," in IEEE Transactions on Industry Applications, Vol. IA-15, No. 2, March/April 1979.

2. R. E. Olsen, "A High Performance Digital Triggering System for Phase-Controlled Rectifiers," Proceedings, 1983 Particle Accelerator Conference, 3/21-23, Santa Fe, NM, IEEE Trans. on Nuc. Sci.

3. F. F. Cilyo, F. E. Mills, and Y. Miyahara, IEEE Transactions on Nuclear Science, Vol. NS-28, No. 3, June 1981.