

OVERVIEW OF THE SPS/LEP FAST BROADCAST MESSAGE TIMING SYSTEM

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Abstract

A fast broadcast message system, also referred to as the general machine timing system, has recently been installed at CERN's Super Proton Synchrotron (SPS). It is used to control the SPS in its roles as a multi-cycling, multi-user service accelerator. The messages are centrally generated by an IBM compatible PC/AT card and broadcast to all users of the system. At the receiving end the frames are decoded and presented to the user in the form of either an interrupt to his intelligent equipment, a hardware pulse or a short message. They are used to synchronise the SPS when used as a 450 GeV fixed target machine, a 315 GeV p-pbar collider, a 100/450 GeV pulsing-coasting machine and also as an injector for the Large Electron Positron (LEP) machine. In the future it will also be used for LEP control. Implementation details and constraints are described, as are experience to date and foreseen expansions.

Introduction

Modern accelerators are widely distributed and diverse groups of equipment which must work in close harmony. It is therefore normal to implement some sort of fast synchronisation circuit as an integral part of their control structure. This paper describes a system which has already achieved limited operational use and is designed for the control of the SPS/LEP machines. The design of the system was strongly influenced by the experience of running the SPS in its various incarnations over the last few years.

Design

The proposal [1,2] for the original timing system of the SPS provided for the broadcast of two groups of 64 unique events to all equipment on the SPS control system. These fiducial markers are set on a clock frame with a 1 msec resolution and are used to relay information about the structure of the accelerator cycle and the manipulations on the beam.

Programable receiver modules establish hardware triggers based on the selection of an event and an optional delay.

From June 1987 the accelerator will be required to operate in a supercycling fashion. The capacity of the old timing system has already been exceeded with the demands of the fixed target, collider and pulsed collider modes of operation and a new timing system is now being commissioned. It can be described as:

- well-timed,
- broadcast,
- short message,
- primarily pre-programmed.

A review of the above points is given later. A few examples of the uses of the SPS system will be described. The first two examples are real in that they have worked in SPS operation with a mixture of the old timing system plus more or less software trickery. The last shows how the new system will be

integrated into the high-level control structure currently being implemented for the June 1987 SPS start-up.

Over 40 timing receiver modules are employed to trigger the low-level RF beam control and acquisition system. It is an example of the "clean" use of the original design. Here, well-understood sequencing of high and low-level control is achieved by timing signals derived from the expected operation of the CERN accelerator complex. These range from "WARNING BEAM" signals from the CPS, the SPS's injector, to "WARNING SLOW EXTRACTION", an internal SPS signal which may, for instance, switch on RF gymnastics to smooth spill structure.

Until the 1986 shut-down turning-off this system was achieved by re-programming individual modules rather than inhibiting the message broadcast. This technique is unacceptable for the more rapid and complex sequencing requirements of supercycling.

A crucial parameter of the CERN proton-antiproton collider facility is the 24-hour accumulation time for one shot of antiprotons. As a consequence injection, acceleration, and storage of this beam demands highly reproducible accelerator conditions and guaranteed monitoring and logging of equipment and beam performance. The antiproton countdown was implemented to force a known sequence of operations to be carried out in a controlled fashion. The sequence used to date comprises three machine cycles, each with unique control actions. The old timing system is capable of delivering the few crucial fast signals (it can for instance signal "WARNING HERE COME ANTI-PROTONS", as opposed to "WARNING TIME OF ANTIPROTON INJECTION") but it cannot send the many other signals required. These - which control running software, check basic readiness and trigger important monitoring and control tasks - are sent over the data links to high-level software. As a result, the operational software is highly coupled both to the details of the timing system and within itself, and the machine control system begins to limit rather than aid flexibility.

From these and similar experiences, we can describe the functions required from the new system. The system should:

- Avoid the conflicting usage from which the old system suffered due to the small number of events.
- Help isolate particular cycles within the supercycle to improve concurrency control.
- Control data gathering with real-time information.
- Tag accelerator data with synchronisation markers.
- Signal the start of high-level tasks which act upon distributed equipment of differing types.
- Enable complex non-periodic cycle changes without the need for receiver module reloading or real-time high-level software actions.

To illustrate these points, we can use the second example above and describe the facilities available to the operations teams which will be provided by the new message broadcast system:

- Specialised messages ("LAST RAMP BEFORE ANTI-PROTON INJECTION") can easily be fitted into the large address space.
- The cycle change possibilities - for example, "store protons" or "store protons and anti-protons" - may be pre-loaded into the message system and branched to as and when needed.
- Physical details - for example, the antiproton intensity requested from the accumulator stack - may be signalled to data gathering and logging processes as the decisions are made.
- Data and control actions may be logged and unambiguously associated, to allow debugging and playback of these costly operations to machine physicists and engineering staff.

General Features

A CERN-wide 1 msec clock is the reference for all machine synchronisation. It is transmitted to all users as a uniquely coded event. Interspersed with these regular 1 msec events are machine related events, viz., start of supercycle, advance warning of injection, etc. The user's timing equipment receives all the timing events and compares them with a pre-loaded subset. From a valid comparison the user module may generate an interrupt to a microprocessor and/or generate a pulse to trigger external equipment. Alternatively it might delay the action for a given number of clock pulses. In both cases the requested action is referenced to the 1 ms clock event.

The message frame

The principal element of the system is the message frame [3]. The meaning attached to the frame caused major problems: finally, the implementation assumes as little as possible and responds according to particular user requirements. The frame is four bytes long, with the first byte defining the subsequent message content. Six types are identified so far:

Type 1. The millisecond clock. The unique first byte is followed by a three-byte modulo 24 number. The number is used mainly for "housekeeping" purposes.

Type 2. The event frame. The bytes showing:

- Message group, e.g. SPS BEAM MONITORING, LEP RF.
- Event name, e.g. WARNING POSITIVE PARTICLE, INJECTION, TRANSITION.
- Cycle type, e.g. PROTON, LEPTON.
- Cycle type number, an identification number of a given cycle type within a supercycle.

Type 3. Cycle count. The unique first identifier byte is followed by a 3-byte integer giving a "supercycle number" serving to tag data acquisitions in a convenient fashion.

Type 4. Time-of-day. Six messages, each with a unique first byte, are used to transmit the Binary Coded Decimal (BCD) values of the second, minute, hour, day, month and year. The last two bytes of each message contain all ones.

Type 5. Concurrency control. The unique first byte is followed by a message defined at run-time by high-level software managers to pass control commands to the control workstations.

Type 6. Real-time information. The unique first byte is followed by conventionally defined bytes containing, for instance, expected beam intensity, data known only just before the message is sent.

To recapitulate the system characteristics mentioned above we can say:

"Well-timed" can be used for machine synchronisation at the millisecond, beam, supercycle and "task" levels.

Sufficient message space is available to control broadcast actions from the generation end, rather than addressing specific receivers.

The terseness of the messages requires consistent use of high-level coding/decoding software.

For efficient use, the majority of the sequencing must be pre-programmed, with well defined break and hold points available. This appears to fall in line with the SPS preference, especially from the operations side.

Signal distribution

In order to reduce cabling costs around the SPS and LEP, an integrated communications system is being installed. This system is based on Time Division Multiplex (TDM) techniques. TDM networks designed according to these Recommendations [4] have been introduced by many PTTs around the world, and equipment is available from a large number of manufacturers. Therefore, it has been decided to base the TDM system for the SPS and LEP on these recommendations.

In the case of the SPS and LEP TDM system, the inter-building physical links will be of two types: optical fibre cable and coaxial cable. Optical fibre cable will be used wherever possible on account of its very high bandwidth. However, the high level of radiation in the accelerator ring tunnels precludes its use in those locations and coaxial cable will be used there instead. Initially, both optical fibre and coaxial cables will carry data at 34 Mbit/sec.

The links provided specifically for the SPS/LEP timing system will normally be configured in a double ring topology, one ring for each accelerator. The links on each segment of the rings are inherently full duplex; this feature is exploited to provide two independently routed signals, following clockwise and anti-clockwise routes around each ring. These alternate signals will be used in the interface equipment for added reliability in case of link failure. It is not however excluded that, for reconfiguration or other reasons, different routes will be used from time to time.

The incoming data streams for the two channels will in general have been transmitted along different physical paths, clockwise and anti-clockwise around the two machines. A path delay compensation circuit, located on the TDM/interface cards, introduces appropriate delays to the channels corresponding to the transmission times of the two paths. This ensures that, in the event of a switch to the alternate channel, the timing signals are not perturbed. The delay circuitry is capable of introducing delays, on the 512 kbit/sec data stream, of any

number of bits between 0 and 255. The value of the delay is set by internal switches on the interface card.

The links used to transport the timing messages operate at 2.048 Mbit/sec. As the timing signals are transmitted at 512 kbit/sec, the extra capacity is used to permit correction of single bit TDM transmission errors. This is done automatically by detecting and inverting isolated zeros and ones in the 2.048 Mbit/sec NRZ signal of the TDM interface unit.

Within each building the timing messages are distributed via twisted pair cables. The signals conform to the electrical characteristics defined by CCITT Recommendations V.11 and X.27 and EIA specification RS-485. Although this standard is designed for multipoint transmission/reception on long bus lines in noisy environments, the d.c. common mode rejection has been substantially increased by the adoption of a.c. coupling on the users' receiver interface.

Master Timing Generator (MTG)

The timing generator card is a single intelligent board which plugs into the IBM PC bus and drives the timing system. It consists of a Motorola 6809 microprocessor controlling on-board (56 kbytes) memory and a number of multi-function registers. The National Semiconductor DP8342 serial transmitter integrated circuit is used to encode the timing message frame. The frames to be transmitted are loaded into the memory and the MC6809 loads them into the DP8342 transmitter at predetermined times. Sixteen external hardware entry points are provided which are used to trigger asynchronous timing messages such as "EMERGENCY BEAM DUMP".

Two other cards, functionally similar to the MTG but based on the much simpler G64 [5] norm, are available: the Fixed Timing Simulator (FTS) is a PROM based card for generating fixed machine cycles, whilst the Programmable Timing Simulator (PTS) permits dynamic message changes. Both are currently being used for pre-installation testing of users' equipment.

Timing Interface

The basic purpose of the interface unit is to receive the timing messages from the multidrop timing line and to pass on the treated data to the timing module(s). The treatment consists of first checking that each Manchester encoded frame received is error free and then converting and stripping the frame down to a four-byte TTL binary coded message.

Two registers are accessible to the users microprocessor, a single byte error register and a three-byte register containing the current supercycle count number. This number will be read each cycle by the IBM PC which generates the timing signals, thus ensuring that the broadcast system is working correctly. For simple applications the interface card can be used by itself. Interfaces exist for the G64, VME and IBM PC standards.

General Timing Modules

The TG3 [6] range of general timing modules are based on a Motorola MC6809 microprocessor controlling an MC6840 triple 16-bit counter (hence the 3).

The TG3 receives SPS/LEP timing messages via an interface and compares each received message with

a set of pre-loaded parameters which are contained in a portion of the on-board memory labelled the event table. The parameters are similar to the transmitted timing messages which consist of 32-bit words organised as four bytes. If a comparison is valid the requested action, associated with that particular condition, is initiated. Normally the action will be to interrupt the user's microprocessor and/or to transmit a trigger pulse to some external equipment.

The TG3 exists in both the G64 and VME standards. Functionally, they are completely compatible.

Conclusions

The major effort in the design of this system has been to eliminate unnecessary assumptions from the implementation whilst providing a wide and flexible service to the user. Thus there is no assumption as to cycle length in the message generator, no requirement of a "start cycle" signal in the receivers. This is no guarantee of success - the "timing" structure of an accelerator is not the whole story - but indications so far are encouraging.

The system was used on the beamline control of the recent SPS oxygen-16 run. This gave a perfect test-bed. Message generation and reception were required to work non-stop for 25 days. Failure would have resulted in no danger to personnel or hardware - simply harassment of the designer.

Since then, many users have made known their requirements, and problems are limited to details of usage rather than inbuilt limitations. These problems will be resolved by current work developing suitable high-level software interfaces. These will harness the flexibility of the system in a well-defined way without compromising it by uncontrolled usage.

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