NEW MULTI-MICROPROCESSOR CONTROL SYSTEM OF THE MAIN RING MAGNET POWER SUPPLY FOR THE KEK 12 GeV PS

S. Matsumoto, T. Sueno, K. Mikawa, M. Toda and H. Baba
National Laboratory for High Energy Physics
Oho-machi, Tsukuba-gun, Ibaraki-ken, 305, Japan

Abstract

The new control computer system has been installed at the last June. The main cpu supervised by the Unix covers man-machine interfacing and correction of current deviation in periodic control algorithm. The two sub-cpu are linked by a LAN and supported by a real time multi-task monitor. The one as the output process controller distributes 15 control patterns to 16-bit D/A converters at every 1.67 ms synchronized 6 phase ac line. The other as the input logs B, Qf and Qd magnet current and voltage by 7 sets of 16-bit ADC at the same clock.

Resulting precision of the currents from beam injection to flat top would be estimated at about a resolution limit of ADC except for current ripple. Ripple currents estimated at several times of an intrinsic ripple in the DCCT.

Introduction

In order to exclude some restriction derived from a pattern by control clock of 10ms and timing control of thyristor bridge of bending magnet power supply, a replacing plan of the control computer system had been started on the system design at the spring in 1983. The design aimed to construct the minimum system in hard- and soft-wares but the maximum in the cost performance to our whole analog and digital hybrid system. The analog control system have to play in main role on real time processes. The digital system is responsible for fast feedforward pattern control and to slow but reliable feedback control loop, i.e. periodic control[1] part of ACR. By control clock of 600Hz, real time part of ACR is carried out by the analog loop with not-expensive cost, because of small systematic current deviation between pattern and measured.

As the result, we proposed for a feasible structure of the control computer system[2] to be constructed reasonably by multi-cpu system. Fig.1 gives the whole hybrid control system.

The main parts of the digital system are constructed from a 16-bit-microprocessor and the family LSI components on a industrial standard bus, and supported by universal operating system as the software bus and standard peripherals, commercially available or compatible by second source suppliers. Under these circumstances, high level language and powerful utilities support development and maintenance of softwares for the flexible pattern control within a reasonable total cost. The main cpu system controls for the slow loop sand supports the other tasks and background jobs. For the fast loop, other cpu systems supervised by a on-line real time multi-tasking OS engage exclusively in tasks of which application programs would be described by assembler.

At that time, H-V90/5 and H-04M would be one of the feasible solutions to construct the multi-microprocessor system with comparatively low cost. Although developing time schedule to both systems were started, but these systems had not been developed.

Multi-microprocessor systemm

Figure 2 shows a layout of the new computer system. The system consists of the main cpu system HIDIC-V90/5 and input and output controller HISEC-04M. The distributed three systems are not hierarchical in software, but rather independent even in assembler level between the main and the controller, because the cpu families are different from each other, especially

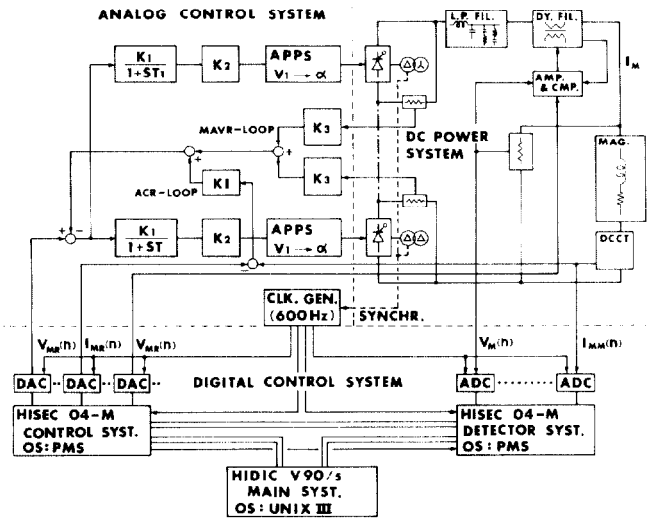

Fig. 1 Schematic whole hybrid control system.

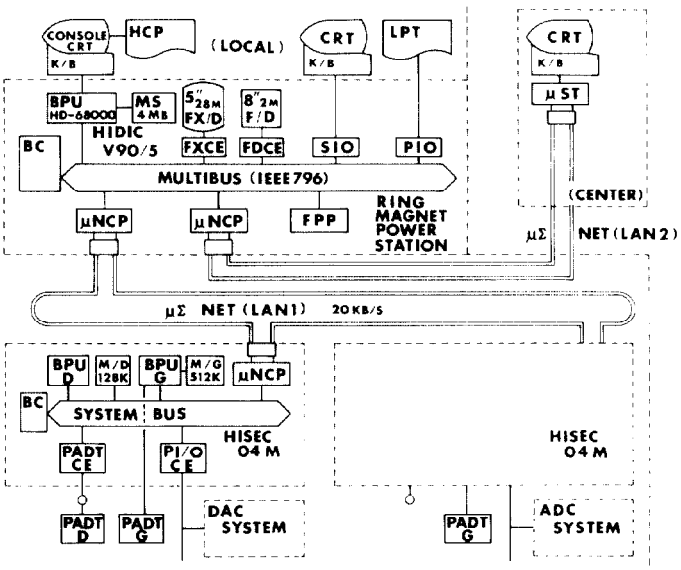

Fig. 2 Multi-microprocessor system.

different memory access in address. The structure supported only by upper version of H-V90 series. The main components are LSI of HD-68000 cpu (second source of MC-68000) and the family. The family of direct digital control system (DDC) as main part of the controller is i-8086 and private LSI modules denoted by BPU/D. In both systems, function module denoted in rectangular block are board circuits with intelligence on the system bus which is compatible to IEEE-796 standard.

H-V90/5 System

Hardware: The system with memory management unit, (MMU), and with DRAM of 4MB on the private bus has floating processor, two loops of local area network based on IEEE 802 (LAN 1 and LAN 2) and standard peripherals (i.e. 5"-28MB hard disc and 8"-2MB floppy disc drive, two stations of CRT terminal, system type-

CH2387-9/87/0000-0689 $1.00 © IEEE
PAC 1987

writer and printer) on the system bus. These resources are supervised by the main OS compatible to the unix system III.

The one of two network-loops, LAN 1, engage in exclusive communication to the input or the output controller because of reliable data transfer. The network transfers pattern or logged data between the main and the output or the input controller by the speed 20 KB/sec in a packet of 512B. The speed is rather slow and correspond to a quarter to the one of H-350 by parallel bus. Moreover, the speed is slower in data transfer by the time sharing OS on the system bus. This is one of bottlenecks for high speed response in fine adjusting injection level of the BPS or tracking offset of QPS.

The one local of the two terminals is supported through SIO in full duplex, but the other remote is forced to communicate in half duplex operation mode only because of micro-sigma network. The terminal is linked by optical cable to the main and is set in the center control room for 12 GeV PS, since the center is about 350m distant from the power station installed the main system. For the sake of derating response of the terminal, the system typewriter works through PIO on the system bus and, therefore, the LAN 2 is private loop of the remote terminal.

Software: The system executes almost of all degital controls except fast realtime parts undertaken by the input and the output controllers and supports developments and file-managements of control programs and data. The application programs will be described in the system language C and FORTRAN 77. The main tasks are the operation controls including start-stop and status monitoring, correction pattern calculation of the periodic control and fine adjustments of pattern data for on-line control. As supporting tasks, the system works on pattern generations, processing of pattern and operation data, control program development, and background processes.

Design principles of these application programs are given.

1. Magnet functions are static or time independent polynomials.
2. Transfer-functions of the magnet systems are described in discrete z-transform.
3. Independent variable is Bℓ, where B and L are flux density and effective length of the bending magnet.
4. In any pattern of Bℓ(n) and dBℓ(n)/dn are continuous at arbitrary n, where n is the n-th control clock from the fiducial point, (PO), of pattern.

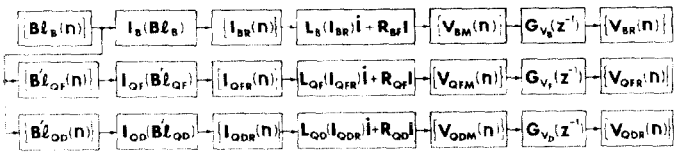

Fig. 3 Algorithm of reference pattern generation.

Fig. 3 gives an algorithm of control pattern generation for reference voltage and current to the analog control system, where (A(n)) denote time serial data file of A(n). $G_{VM}(z^{-1})$, M=B,QF,QD, are inverse transfer functions from the reference pattern voltage to magnet input voltage.

$$I_{MR}(n) = \sum_{k=0}^{mI} a_{MIk} (Bl(n))^k$$

$$L_M(n) = \sum_{k=0}^{mG} a_{MLk} (I_{MR}(n))^k$$

$$G_{VM}(n) = \sum_{k=-1} a_{VMk} V(n+k)$$

M=B,Qf,Qd.

$$B'\ell_{Qm}(n) = k_{Qm}(n) B\ell_B(n)$$

For BPS, reference voltage pattern is divide and distributed to the reference voltage of 12 pulsed thyristor converter groups in accordance with the desired voltage to minimize generation of reactive power.

Fig. 4 shows an algorithm of the periodic control

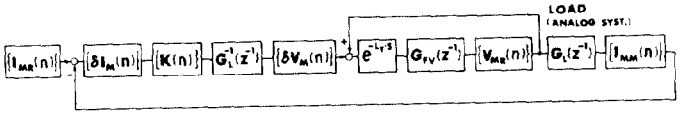

Fig. 4 Algorithm for periodic control of magnet current deviation.

of current, where $G_L(z^{-1})$: inverse transfer function from reference voltage to excitation current,

$\delta I_M(n) = I_{MR}(n) - I_{MR}(n)$, M=B,Qf,Qd

$G_{FVM}(z^{-1})$: transversal finite impulse response low pass filter,

(k(n)): gain file of periodic control,

$L_T = m \cdot T$: dead time of m times period T, m: integer.

These function files are used for fine adjustment of injection level of the bending magnet without tune shift and corrections calculate in the same algorithm of the pattern generation.

There are tracking offset calculations in the similar situation at injection correction, that is, by given or calculated offsets correction of reference voltages are computed in the same scheme as pattern generation.

Man-machine-IF: Main parts of the programs are described by the FORTRAN and subroutines by the FORTRAN and the C. The programs make on a CRT of terminals parameter files to communicate with control programs. Powerful utilities of the unix are very useful not only program developments but also maintenance of the application programs, controlling and monitoring the whole system by file management, screen editor and shell command etc., as long as slow response (a half minute or more) is allowable. However, fine adjustment of injection or tracking is required higher response. These programs would be optimized and sophisticated less than a half minute.

Controller System

On the same system-bus, the controller of H-04M/DG type is divide by two sub-system, BPU/D and BPU/G, of which microprocessor are quite different families, i-8086 and HD-68000. The one works as DDC and the other is a data processing or supporting system to the DDC. On the system bus of the DDC, BPU/G has a memory window of 16kW, by where the data are mapped on the g-mem through MMU. The system be able to access d-mem and PIO fixed address on the bus. In our case, the system engages in communication through LAN1 with V90/5 and read or write data or message on the d-mem.

BPU/D-out: The system is DDC and has 64kW (p-mem) for program memory and 32kW (d-mem) for data memory as application area. These memories are DRAM backuped by battery. On the system, process monitor system, (PMS), is released as on-line real time multi-tasking OS and problem oriented language, (POL), as a developing tool of macro-assembler level for an application program. By POL, a program development execute graphically in similar to ladder sequence on the program and debugging

tool, (PADT), at off-line mode.

The output BPU/D controlled by PMS execute for application program as tasks, i.e. start-stop, PO process and sampling synchronization etc. Routine output processing distribute to output 15 pattern data in d-mem through PIO to 16-bit DA converters, timing pattern of by-pass thyristor for bridge control of BPS and pattern timing signal to handle the beam, PO,P1,P2, P3,P4, etc, as shown in Fig. 5.

DAC: Nine sets of DAC work for BPS, that is, six of them serve as reference pattern voltage of the thyristor converter group, two as the dynamic filter detector and one as the reference current for the analog ACR. Figure 1 shows schematic relation among these hybrid loops for one group 12-pulse converter of BPS, the horizontal focusing and defocusing magnet power supply, Q_fPS and Q_dPS. In the Q_f and Q_d, respectively, two sets serve for reference voltage and current to the analog loops and one set for dynamic filter.

The system outputs these pattern data to the fifteen sets of DAC in every clock of 1.67mS. But the data convert in synchronizing to the zero-cross pulse of six phase ac power line. Thyristor bridge control signals of by-pass and gate suppress are distributed to working bridges by the system. However, when these control data are output through PIO insulated by photocouplers, jitters among bits of a PIO and among PIOs are not able to neglect compare to 600Hz. We have been used DAC with buffer resister and conserve the synchronism between analog signal and the clock. However, the timing signals of the bridge control through PIO are driving Hg-relay and, by the contact signal, pulse amplifiers excite ignition pulses to thyristor gates. Because the delays plus jitters of Hg-relay are several times of the clock, synchronism between the control signal and the clock are forced to couple loosely, but synchronism among bridge control signals are carried out severablly in hardware.

BPU/D-in: The input controller system is the dual with the output controller as long as hardware and system soft, except digital input and output. The BPU/D works on the time interval between PO and P5+t0 from output-BPU/D. t0 is one of parameters at pattern generation. The main task is to collect the data of ADC through PIO and to accumulate and save at every control clock the data to the d-mem. After accumulation of the data up to a given number of pattern period, sampled data are accumulated in another buffer memory area of d-mem alternatively.

ADC: At every sampling clock, the system reads data of seven sets of 16-bit-ADC with a sample hold amplifier. Three sets serve for the DCCT current signal and the other for the dc voltage applied to the B-, Q_f- and Q_d-magnet in the same clock of the DAC system. The clock synchronizes zero-cross pulse, but has a constant lag of about 100 microsec which is about 2 times of the conversion time. At the edge of sampling clock pulse, ADCs have ceased their conversions because they had started synchronizing to the zero cross pulse. DCCT current data of these serve in the periodic control loop for calculation of corrections to the reference voltages.

BPU/G: The system has the OS of the on-line, PMS, for real time multi-tasking and the OS of the off-line, CP/M-68K, for program development and debugging. The system supports a subset version of FORTRAN 77 and C as the program developing language on the CP/M-68K. The developed program of object level is converted to the program of PMS by released utilities. Therefore, source programs of task are described by C-language.

The main tasks of BPU/G are sending and receiving of pattern data and message between V90 system through LAN 1, start-stop and loop-check routine in the input and output controller.

Performances

The V90/5 system was introduced in at the April 1985 and the H-04M were settled in the site at the October of the same year. After preliminary installation of the system, we had some problems to be overcome for a routine operation of whole system, i.e. common mode noises in the digital and analog loops, precision of magnet and transfer functions, synchronization between the input and output controller, and slow response of the main systemand of communication loops. considerable parts of them have been removed. Stabilities and reliabilities of the whole system have been sufficient level for the operations. The new system serves in the routine operations without any trouble, since the first run of this year. Detailed processes of optimizations or improvements on these will be write somewhere.

As an example, Fig. 5 showes typical current deviations of B-magnet. On the injection, points form four or six lines derived from ripple current. The spacings of these lines would be estimated as 45mA correspoded to the bit resolution of ADC (3kA/10V). The p-p deviation on the injection agree to the intrinsic ripple of the DCCT.

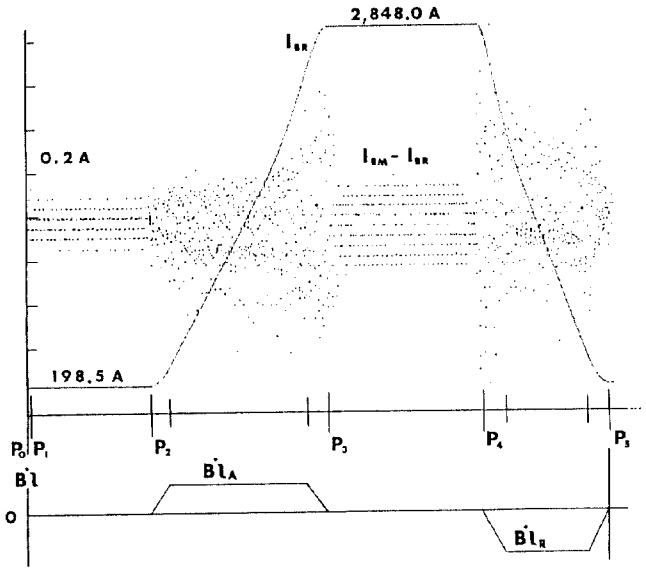

Fig. 5 Typical bending current pattern, measured current deviation on a routine 12GeV operation, (upper side), pattern timing pulses P_k, and Bl pattern, (lower side).

Acknowledgements

The authors would like to express their sincere thanks prof. Michio Nakano (Tokyo Inst. Tech.) for his discussions and many advices on the control system. The would like to describe their thanks to professor Emeritus T. Kamei for his encouragements and supports. They would like to say their glatitude to director Prof. M. Kihara for his advices. They are much indebted to prof. K. Muto for his discussions on the system construction, prof. N. Kumagai for his determination of magnet functions and of operation points at the system tunning, and prof. M. Kondoh for his discussions on the project and to many colleagues of PS group for their discussions and collaborations.

References

1) T. Inoue et al., Contl. Sci. & Tech. for Prog. of Soc. (IFAC 82) vol. 6, 3137, Pergamon Press (1982).
2) S. Matsumoto et al., Proc. 5th symp. on Accel. Sci. & Tech., Tsukua 1984, 223 (1984).