RECENT DEVELOPMENTS IN THE TRIUMF CONTROL SYSTEM

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INTRODUCTION

The principle ideas and underlying architecture of the TRIUMF Central Control System have not changed since its commissioning in 1974. As described elsewhere[1,2,3] the system consists of a number of Data General minicomputers which communicate using a proprietary Data General parallel direct memory access interprocessor bus, and which share access to a common multiported memory containing a limited descriptive data base of device addresses and pointers to acquisition and conversion routines (Figure 1). The most important idea of the TRIUMF Control System design, and one which has in large measure determined the manner of its evolution, is the use of the executive crate, by means of which all central system computers share direct and immediate access to the entire seven parallel branch CAMAC system, which in turn interfaces all accelerator devices and most of the main Control Room console devices. Expansion of the Control System to date has been realized on one hand by the addition of CAMAC crates, and on the other by the addition of minicomputers to the executive crate interface. With the use of active extenders, the executive crate has been extended to three CAMAC crates, and could in principle electrically support as many as 1500 sources. In practice, this number is limited to about 30 sources by bandwidth considerations, and to even fewer by the geographical requirement that sources be located physically within about 50 ft. (I/O bus length limitation) of the executive crate.

This paper describes three recent developments in the TRIUMF system whose designs have been influenced by its multisourced architecture. These are:

1. The introduction of a Qbus computer to the executive crate;
2. The development of an STD-based multiplexed ADC system with an interface to CAMAC; and
3. A control subsystem for the TRIUMF Third Ion Source using a CAMAC serial highway and a commercial Programmable Logic Controller.

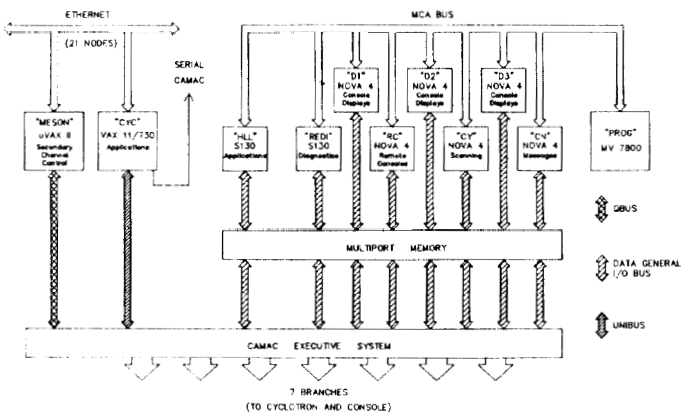

Figure 1: The TRIUMF Control System

1. Executive Crate Q-Bus Interface

The modularity of the executive crate approach, in which the computer I/O bus specific component is in a single module separate from the CAMAC branch drivers and the arbitration, has permitted the easy addition of VAXes to the executive crate, which now share access to the CAMAC system with the Data General minicomputers. Application of a VAX 11/730 for accelerator development has been reported elsewhere.[4]

Recently, a micro-VAX II has been added to the central system to control secondary, or pion, beam lines. Control of these beam lines is done by experimenters from data acquisition areas. The centralized approach was chosen for a number of reasons. Device controllers were already located in the central CAMAC system, and leaving them was both easier and more economical. Moreover, that choice allowed retention of an existing redundant secondary beam line control system using existing control system facilities. Secondly, the centralized approach, which gives direct access to accelerator parameters such as beam energy, intensity, polarization, or others which may be required by operators of secondary channels, eliminated the need to devise a communications network and protocol to the central system. Finally, interfacing centrally made the choice of a VAX for secondary beam line control economically realistic, and that in turn gave access to the site Ethernet LAN running DECNET, and thereby simple communication with experimental data acquisition systems.

The Secondary Channel control micro-VAX II was interfaced to the Executive Crate using the QBus System Crate Interface SCI 2280 from Creative Electronic Systems. This is a memory mapped interface, and CAMAC cycles are therefore terminated if they last longer than the micro-VAX Q Bus timeout, which is approximately 10 μsecs. Unlike earlier Q and Unibus computers, this timeout cannot be extended. The parallel branch to the secondary beam line crates is over 300 m long, and includes two pairs of differential branch extenders. Cycles addressed to those crates last approximately 11 μsecs, and may last longer if executive crate arbitration is required. Consequently, micro-VAX originated CAMAC cycles for secondary channel control frequently time out, taxing CPU resources doing repetitive cycles and timeout recovery sequences. The System Crate Interface has been returned to the manufacturer for modification. The micro-VAX will no longer wait for completion of the requested CAMAC cycle. Rather the QBus cycle will complete upon initiation of the CAMAC cycle, and a flag, data, and status will be latched in the interface on cycle completion for subsequent testing by the VAX. The solution proposed by the manufacturer requires expanding the System Crate Interface to double CAMAC width.

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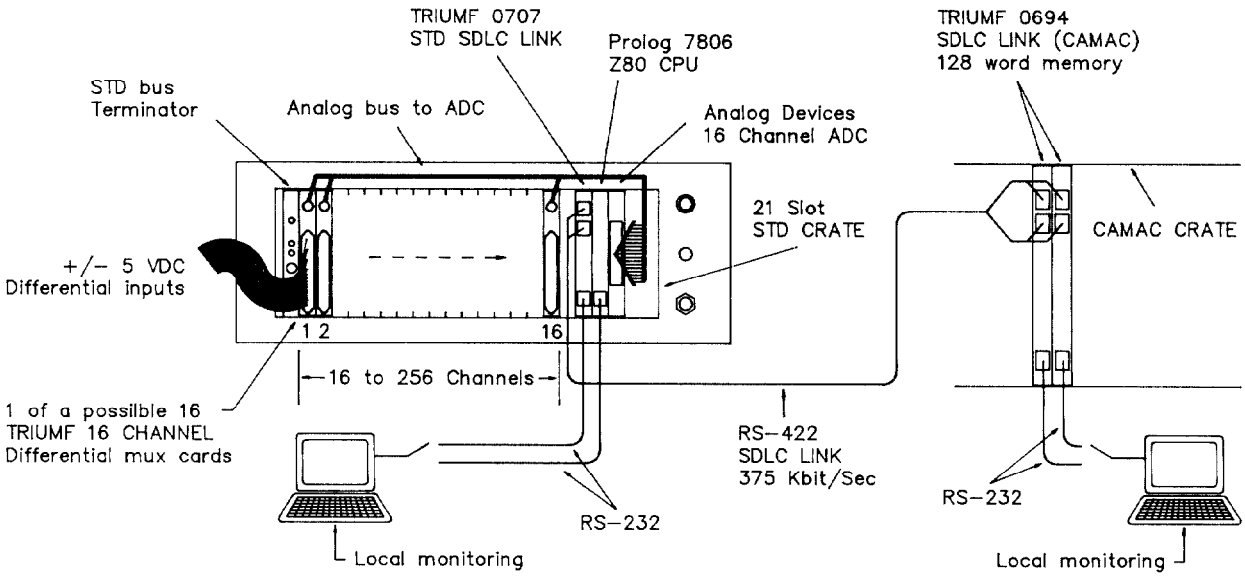

Figure 2: An STD-based multiplexed ADC System

CAMAC Memory and Communications Module

In any multisourced system, it is desirable to use CAMAC modules whose normal function requires only a single cycle to execute. To prevent interference between computer sources, or even different tasks within one computer, a module requiring more than one cycle needs a reservation flag which adds a two cycle, or up to 50%, overhead. For this reason we have made extensive use of a 128 word CAMAC memory, any of whose 24 bit words may be randomly accessed with a single CAMAC cycle by using three function code bits in addition to the four subaddress bits to provide a seven bit "address".

Recently we have introduced a dual-ported version of this CAMAC memory which provides fast transparent CAMAC-CAMAC communications in a single width module. The module is normally used in pairs. Any data written from the CAMAC dataway to a location in one memory is transmitted transparently to the same location in the other. Communication is bidirectional, and higher level software must insure that conflicts do not arise due to the same location being written from both sides.

The CAMAC memory/communications module can communicate using either RS422 twisted pair or a fibre optic link, switch selectable. Both physical links use the SDLC protocol controlled by an Intel 12 MHz 8344 SDLC microcontroller. Data written to one memory from its dataway port are also stored in a 512 byte FIFO which is scanned for new entries by the 8344 controller, and then transmitted.

Although intended primarily for use in pairs, in which case communication is at the rate of 375 kbits/second, a system of up to 15 stations can be configured, with each secondary station passing on received messages to a specified destination. Module and destination addresses are DIP switch selectable. When operating with the RS 422 link the module can be bypassed using a front panel switch. In this case, it no longer responds to link commands until a "reset" is issued, either by a front panel switch or a dataway command.

On power up or reset the module does a self test of internal memory, setting a testable flag if an error is detected. The CAMAC memory is not affected. A number of CAMAC function codes are available for diagnostic purposes and the memory can be examined locally using a monitor attached to a front panel RS 232 connector.

Standard Bus (STD) Multiplexing System

An economical STD-based system has been designed for conversion of analogue signals where they occur in high density. STD was chosen for compactness (254 channels in a 7 inch high, 19 inch rack mounted crate) and economy (about $16 US/channel, excluding CAMAC). The system communicates with the CAMAC memory/communications module described above to provide single cycle random CAMAC access to up to 254 (in two modules) channels. (Two channels are reserved for use as watchdog counters.)

The system is shown in Figure 2. It consists of from one to sixteen TRIUMF-designed multiplexer cards of sixteen channels each; a commercial sixteen channel ADC; a commercial Z80 processor board; and a TRIUMF designed STD communications module linked to the CAMAC memory/communication module.

The STD multiplexer cards accept 16 bipolar 0 to 5 volt differential input signals. Input is filtered, and protected to 70 volts. The selected channel is buffered, and a single ended signal is passed to one channel of a 16 channel, 12 bit (two's complement) Analog Devices RTI 1260 ADC.

A Prolog 7806 Z80 processor controls signal switching, and puts the digitized results into the memory of an STD memory/communications module. The front end of this module is identical to the CAMAC memory/communications module, with which it communicates. SDLC transmission rate, using either RS 422 differential twisted pair or fibre optics, is 375 kbits/second.

The system scans at the rate of 3200 channels/second, or 254 channels in 80 ms. Once a day, and on power up, the processor shorts the inputs to each multiplexer card, and measures the zero offsets. These values are stored and subsequent readings corrected. If the measured offset becomes too large, an error flag is passed to the control system, and a front panel LED indicator is lit.

The system can be locally monitored by attaching a terminal to the RS 232 port of the Prolog processor. Raw offsets and data may be displayed in decimal, octal or hexadecimal formats, or as voltages. Off scale channels are indicated, and the watchdog counter is also displayed. This display disables itself automatically after a few minutes, and may be restarted by typing any key. When the display is enabled the program outputs one line to the terminal after each complete scan, lengthening the scan time for 254 channels to 270 μsecs (assuming a 9600 baud terminal connection).

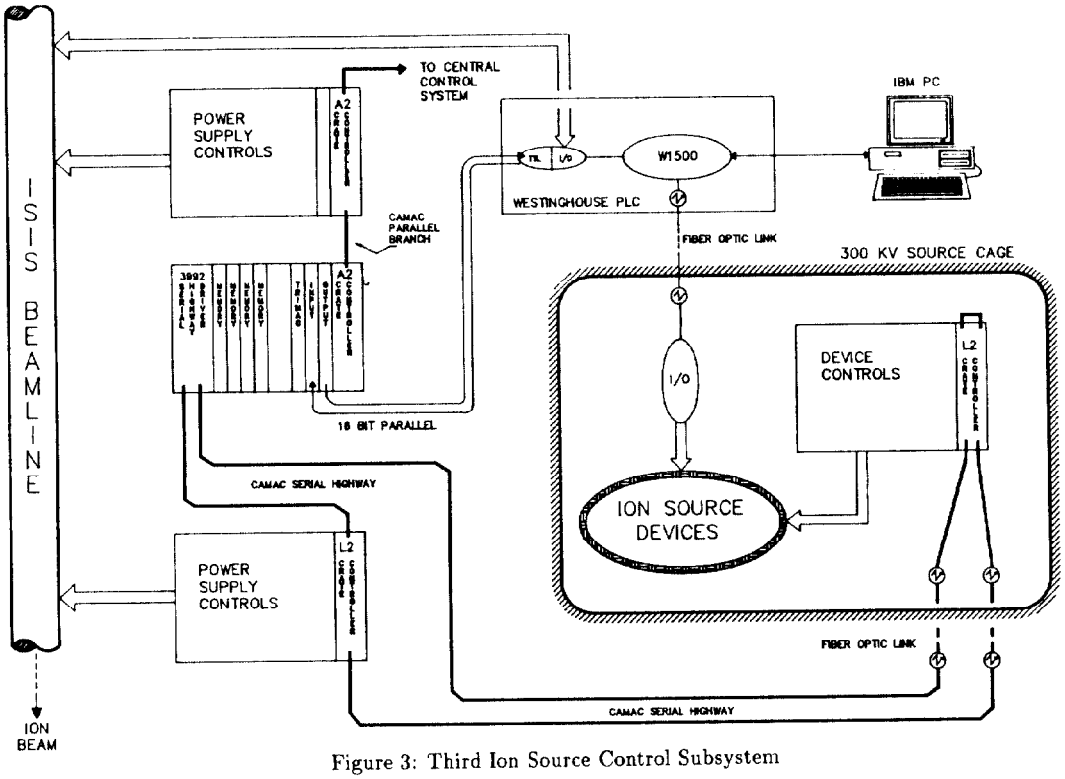

Figure 3: Third Ion Source Control Subsystem

Third Ion Source Controls

The first application of the Standard Bus Multiplexing System has been in the control system for the recently installed high intensity CUSP H^- Ion Source. This system (Figure 3) also makes use of a commercial Programmable Logic Controller for digital control and interlocking, and of a serial CAMAC highway—both new developments at TRIUMF.

The serial highway was necessary primarily because the parallel branch in the Ion Source area could accommodate no more crates. The option of driving the serial highway directly out of the executive crate was excluded for reasons of economy and because the longer serial highway cycle times would adversely impact the performance and timeout settings of the parallel branches. For these reasons the branch is driven by a Kinetic Systems 3992 Serial Highway Driver which resides in one of the central system parallel crates. It operates bit serial at 5 MHz. Fibre Optics is used to reach the Ion Source cage, which is at −300 kV.

Because multiple parallel CAMAC cycles are required to initiate a single cycle on the serial branch, a reservation module is required. This means a total of nine cycles is required to achieve a single dataway operation in a serial crate. This is 50% worse than for the TRIUMF designed serial link which is already in use for two other TRIUMF Ion Sources, but has the advantage of being standard CAMAC.

Another difficulty occurs when a crate is bypassed or goes off line. Tests to determine whether a crate is on line again, or to initialize a crate, require special cycles lasting up to 250 ms. This affects not only the computer responsible, but any other which is doing a normal cycle on the serial highway. For this reason, automatic reinitialization has not been implemented for the serial highway as it has for all parallel branches, and an operator initiated procedure is required.

Nonetheless, it is our intention to extend the serial highway to all three Ion Source Faraday cages, and consideration is being given to adding a new serial highway for secondary channel control.

While analogue control and readback in the CUSP Ion Source cage uses the serial CAMAC highway, all digital control, readback, and interlock logic is done by a commercial Programmable Logic Controller (Westinghouse PLC). The processor is located at ground potential, and a fibre optic communication link to its I/O modules was developed to bridge the 300 kV gap.

In addition to performing logic, the program in the Westinghouse controller passes digital status along with an address from a 16-bit output register to a CAMAC 16-bit input register. A TRIUMF designed intelligent auxiliary crate controller puts this data into four 128 word CAMAC memories, making it available to all central system computers. Commands from the central system are passed to the Westinghouse controller for execution in the reverse way.

At present, the Westinghouse Controller has 800 input bits and controls 200 output bits. Its program loop executes 450 equations in 68 ms, including communication with the central CAMAC system. It is our intention to expand the use of this system to include digital control of a fourth ion source, soon to be added to the same 300 kV Faraday cage, and to more ground potential digital control points.

References

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[4] D.A. Dohan and M. Mouat. "High Level Extensions to the TRIUMF Control System." To be published in the Proceedings of the Eleventh International Conference on Cyclotrons and Their Applications.