A PRECISION PULSER FOR MAIN RING EXTRACTION

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Summary

A pulser has been designed to produce a 14 Hz sinusoid current pulse at a 2 s rate with peak amplitudes from 400 amps to 3750 amps, and a long term stability of ±400 mA. Short term stability is achieved by the use of a precision voltage regulator for the capacitor bank. This voltage regulator uses gate turnoff thyristors to control the charging current to the 13 mF capacitor bank. Load current is monitored with a precision dc current transductor. The peak value is read into a single chip microcomputer programmed to act as a digital regulator. The microcomputer calculates reference values for the capacitor bank charging supply and the capacitor bank voltage regulator.

Introduction

A vertical bend of 33 mrad is required to steer particle beams between the Main Ring and the P-bar transport line. This is provided by a string of two Lambertsons and two C magnets. For P-bar injection, a conventional 20 V, 500 A dc power supply powers the string. For 120 GeV extraction to the P-bar target, the magnet string is pulsed to the appropriate current.

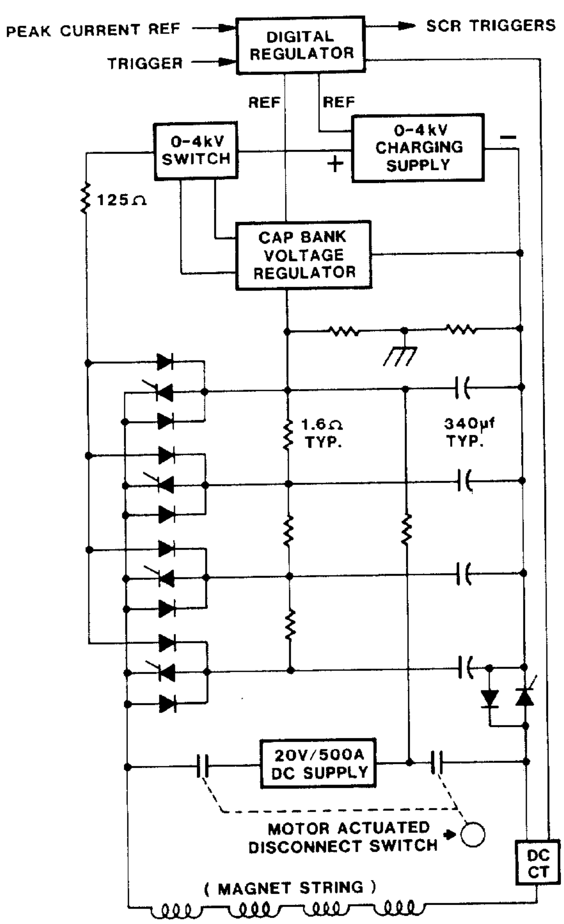

Figure 1. Basic Pulser Configuration

*Operated by Universities Research Association, Inc., under contract with the U.S. Department of Energy.

This prevents the fringing fields of the Lambertsons from distorting the main ring injection orbit and reduces the power losses by a factor of 24 for a pulse rate of once every three seconds.

Basic Pulser System

The power supply system shown in Figure 1 can be subdivided into five interrelated components; a pulser which produces a high current sinusoid into the magnet string; a capacitor bank charging system to provide the initial energy for that pulse, a digital regulator to measure the load current pulse and make the necessary correction to the capacitor bank voltage, a dc power supply and isolation switch to provide magnet current for P-bar injection; and finally an interlock and control system to coordinate the activity of the various components with the outside world.

The pulser is a conventional resonant discharge type in which energy stored in a capacitor bank is transferred into an inductive load thru a thyristor switch. Typical voltage and current waveforms shown in Figure 2 indicate that a full cycle of voltage and current is executed.

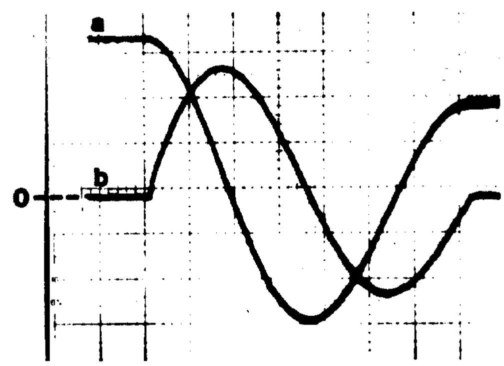

Figure 2. a. Cap Bank Voltage 800 V/div
b. Load Current 1 kA/div
Sweep = 10 mS/div

Energy is recovered in the capacitor bank by letting the load current reverse (instead of using a separate recovery choke). Relevant data for this pulser is listed in Table I for operation at 120 GeV.

load inductance	9.6	mH
load resistance (dc)	40	mΩ
(ac)	125	mΩ
capacitor bank	13	mF
resonant frequency	14.3	Hz
peak load current	2800	A
initial voltage	2800	V
initial stored energy	51	kJ
losses per pulse	34	kJ

Table I.

The capacitor bank consists of 4 individual sections each consisting of three 1080 µF units. This is done to minimize the damage resulting from the fault of an individual unit. As can be seen from Figure 1, one side of all sections is tied to a common bus. Each section, however, is charged thru an isolation diode and discharged by a series pair of thyristors paralleled by a series pair of recovery diodes.

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Capacitor bank sections are also coupled by 1.6 Ω resistors, which serve to passively discharge any section not normally discharged by its thyristor. Should a thyristor fail to conduct, it would be forced to block the sum of the initial capacitor bank voltage and the reverse voltage during the recovery part of the cycle if these resistors were not present. The voltage on the capacitor bank is balanced with respect to ground. Thyristors on both sides of the capacitor bank sections isolate the magnet string from the supply except during the pulse. This differential configuration reduces the noise generated by the sudden application of voltage to the load.

Capacitor Bank Regulation

The capacitor bank charging system must provide the initial voltage on the capacitor bank and also make up the losses in the system. This requires a voltage regulated current limited dc power supply the output of which is referenced 400 V higher than the capacitor bank initial voltage. The output of this supply is connected to the capacitor bank through a gate turnoff thyristor (GTO) switch and series resistor. A capacitor bank voltage regulator turns the GTO switch on and off to maintain the capacitor bank voltage at a given value.

The heart of the charging system is the capacitor bank voltage regulator. The regulator which is referenced to the common side of the capacitor bank receives its reference as serial data via an optical link from the digital regulator. Each reference transmission includes a flag to disable the regulator for the duration of the pulse. A 14 bit DAC converts this reference to an analog value which when compared to the actual capacitor voltage in a precision analog comparator, provides signals to control the GTO switch. If the reference exceeds the capacitor voltage, the GTO is pulsed off. Should the capacitor voltage fall below the reference, the switch is pulsed on. With such a system, the hysteresis of the comparator determines the regulation of the capacitor voltage. Typically, this is 0.5 V.

The GTO switch is designed to block a voltage equal to the sum of the charging supply output voltage and the peak negative excursion of the output pulse voltage which is on the order of 5.5 kV and to interrupt currents up to 10 A at a 4 to 6 Hz rate to meet the regulation requirements of the system. It consists of a compensated series string of 9 - 25 A devices.[1] A positive gate pulse turns the devices on while a negative gate pulse causes them to block. Unlike a thyristor, the current gain of these devices is on the order of 2 or 3; therefore, a gate current, particularly the negative pulse, must be 4 to 5 A for reliable operation.[2] The GTO gate pulser uses a thyristor to discharge a capacitor into the gates through an impedance matching isolation transformer. Both positive and negative pulsers share the same transformer.

Digital Regulator

The digital regulator is based on the Motorola 68701 microcomputer chip which includes 192 bytes of RAM, 4096 bytes of EPROM, and a host of other features.[3] Program parameters for changing the performance of the regulator are downloaded from PROM upon initialization and may be modified via front panel switches. A hexidecimal display facilitates the examination of the contents of RAM for diagnostic purposes.

A monitor routine checks the status of the power supply system according to the flow chart of Figure 3. If the dc power supply is on for 8 GeV operation, the regulator reads both the reference and load current, calculates the integral of the error voltage and outputs the result as the power supply reference. This routine cycles at a 2 s rate. If, however, the pulse power supply is on for 120 Gev operation, each trigger generates an interrupt which cycles the program thru the pulse regulation routine. This routine sequentially disables the capacitor bank voltage regulator, triggers the pulser, then waits for the peak value of the pulse to occur. The peak value is read, subtracted from the reference, and the result used to calculate the reference for the capacitor bank voltage regulator in a manner similar to that used for the dc power supply. Following the current pulse, the routine enables the regulator to recharge the capacitor bank. Load current is monitored by a 5000 A Holec precision CT which has a stability of 50 ppm in our environment and a bandwith of 10 kHz.

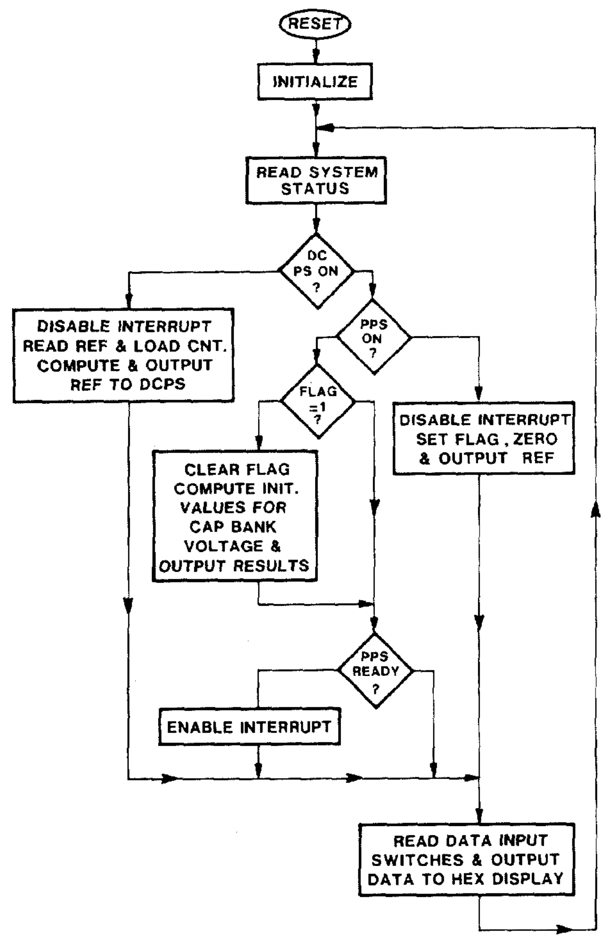

Figure 3. Software Flow Chart

Interlock and Control

For 8 GeV operation, a conventional dc power supply powers the magnet string. For pulse operation, this supply must be safely isolated from the load. Our approach was to build a motor-driven high voltage knife switch. A commercial linear actuator with a 4 inch stroke moves the switch blade. This switch is an integral part of the interlock and control system (ICS) since dc and pulse operation are mutually exclusive. Once a particular power supply mode has been selected either locally or remotely, the ICS checks if the load current and the capacitor bank voltage are zero before energizing the switch. Only when the switch is fully open can the charging supply be energized and only when it is fully closed can the dc supply be energized. Once either of these supplies is on, the primary power to the switch is removed. The ICS also monitors the status of the various elements of the system for both local and remote display.

Improvements

The power supply in its present configuration is operating with a charging supply which has only a 6 A capacity so the repetition rate is limited. A 15 A replacement is under construction which will bring the repetition rate up to design value. The pulse to pulse stability appears to be on the order of .05%. Fine tuning of the pulse regulation routine parameters should result in a significant improvement in this.

References

1. Hitachi GTO Thyristor, Pub. No. SD-E701A, Hitachi, Ltd.

2. H. Fukui, et al., "Switching Characteristics of a Gate Turn-Off Thyristor", unpublished

3. MC6801 Reference Manual, Pub. No. MC6801RM(AD), Motorola, Inc., 1980