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A 28 kV ± 0.020% 200 kW DC POWER SUPPLY*

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Abstract: Design, construction and testing of a prototype HV power supply for the klystrons of the 300 MeV racetrack microtron (MUSL) of the University of Illinois are described. Regulation of 0.02% is achieved with three voltage feedback loops. Two loops to thyristor phase control circuits on the ac primary of a 12-phase rectifier transformer regulate its output to within ± 0.2% (line regulator). A third loop controls a series-connected tetrode to bring the output to within ± 0.02% of the preset value. The voltage drop across the tetrode can be set between 800 V and 1600 V; this setting is maintained by one of the loops to the line regulator. Other unique features are protective circuits that limit the fault current to 150% of the rated current when the klystron and/or the tetrode spark over. Voltage spikes generated by the thyristors are attenuated with LP-filters.

Introduction

The frequency and power output of the klystrons for the MUSL's rf system are very sensitive to dc plate voltage variations. A 28 kV 7 A power supply, regulated to ±0.02% is required. A prototype power supply was designed, built, and tested at Argonne National Laboratory. The power supply is designed for an output range from 0 to 28 kV. Taps on the rectifier transformer primary (50%, 75%, 100%), reduce ripple and improve power factor for operation much below 28 kV. The ac input to the high voltage (HV) rectifier transformer is controlled by thyristors with two feedback loops. One loop controls the HV dc output, the other loop maintains the voltage drop across the tetrode series regulator to a preset value between 800 V and 1600 V to ±0.2%. Unique protective circuits respond within μs to certain fault conditions.

Overall Circuit Description

The simplified diagram of Fig. 1 shows the major components, the regulator control loops, and the fast-fault shutdown logic for the power supply.

The 480 V 3-phase power is connected to line filter FL1 through a manually operated circuit breaker CB1. The filter attenuates communtation spikes of the phase-controlled thyristor switch S1 before they reach the incoming line. The power supply is energized with the closure of main contactor K1 and the gating-on of S1. The damped filter FL2 is used to reduce commutation spikes caused by S1's operation on the output of T2. The output of rectifier transformer T2 is adjustable from zero to maximum by means of phase control of S1's gate signals. The two HV secondaries of T2 are rectified by 3-phase full-wave diode bridges, BR1 and BR2. The dc output voltage of the series connected bridges is controlled by the feedback loop to the line regulator. A damped low pass filter comprising L, C1, C2, and R2 reduces the ripple voltage.

The filtered HV is applied to the series regulator. During normal operation, the voltage drop across the tube is maintained by the line regulator with feedback from the differential sum of the voltages on the cathode and anode of the tetrode and a preset reference voltage.

The power supply's output voltage is controlled by an error amplifier that compares a reference voltage V2, set by a 14-bit digial-to-analog converter (DAC) with the power supply output. The voltage error is converted to a frequency and optically coupled to the HV deck where it is converted back to a voltage. This error voltage controls the tetrode.

The output power is passed through a saturated time-delay transformer (STDT)[1] and branched to the two klystrons, each having a dc ampere meter with overcurrent trip settings.

Three Loop Regulator

The regulator circuits will be described in more detail with reference to Fig. 2.

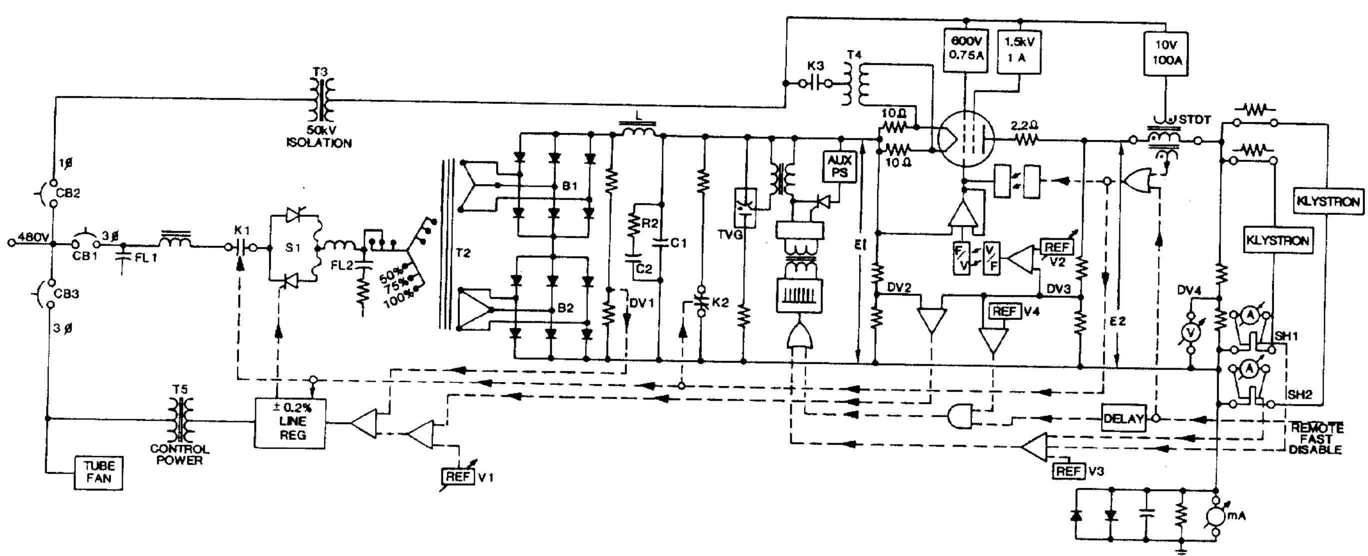

Fig. 1 Power supply one line diagram.

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Constant Tetrode Voltage Drop Loop: The function of this loop is to hold the tetrode cathode-to-plate voltage relatively constant during programmed increases of output voltage E2 and during steady-state

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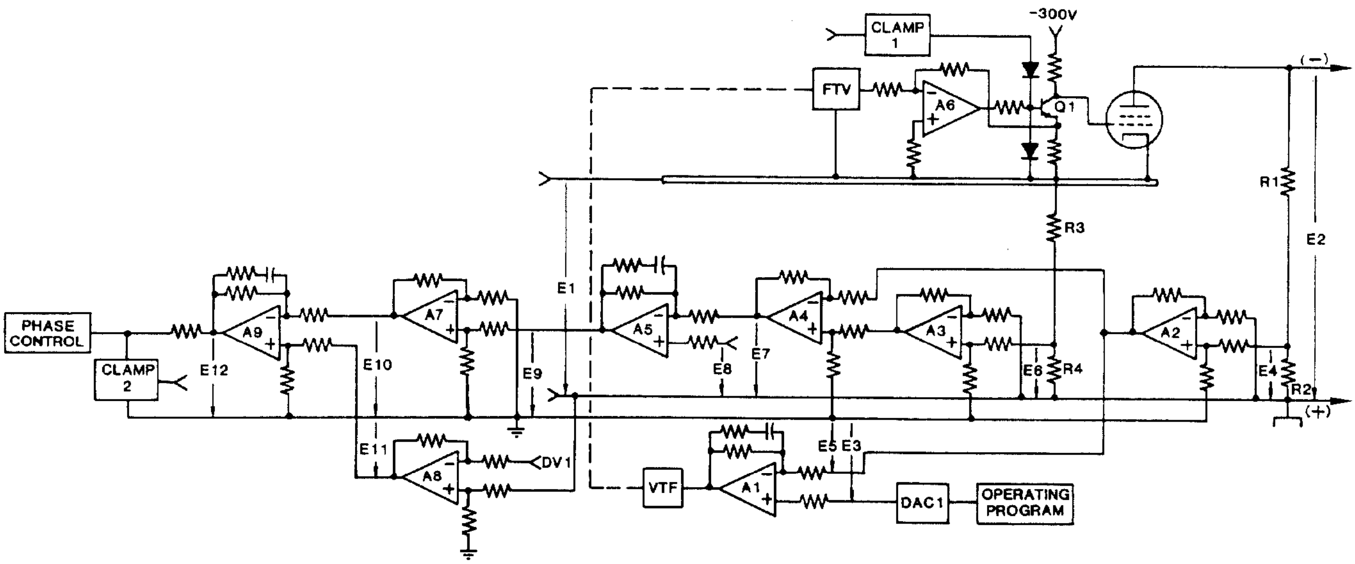

Fig. 2 Three loop Regulator.

conditions. It samples input voltage E1 and output voltage E2 and references them to ground with amplifiers A2 and A3. After being differentially summed in amplifier A4, the sum is compared in error amplifier A5 with the reference voltage V1 yielding an error signal E9.

AC Line Regulator Loop: Error voltage E9 is buffered by amplifier A7 and applied as reference voltage E10 for the line regulator to differential amplifier A9. A signal from the voltage divider DV1 (Fig. 1) is buffered and referenced to ground by differential amplifier A8. This signal is applied as feedback voltage E11 to amplifier A9. The output of A9 is the input to the phase control circuit which programs the thyristor firing angles of the 3-phase full-wave switch S1. The loop gain of A9 forces S1's phase control to bring the rectified ac voltage, represented by E11, to within 0.2% of voltage E9.

Output Voltage Regulator Loop: Output voltage E2 is compared with a reference voltage set with DAC1 by amplifier A1. Its error signal controls the grid of the tetrode and the combined loop gain of A1 and the tetrode maintains E2 within ±0.02%. Since there is a ~ 28 kV voltage difference between A1 and the tetrode, an optical, frequency-modulated link is employed. Analog signals are digitized by a voltage-to-frequency (VTF) converter operating over a frequency range of 0-1 MHz, prior to fiberoptic transmission, and then decoded to analog levels using a frequency-to-voltage (FTV) converter.

Regulator Clamps: Due to the need for fast shutdown of the tetrode, a clamp circuit (clamp 1) was installed on the base of Q1. This circuit is diode-OR'ed with the program voltage from the FTV converter. It applies a +13 V signal to the base of Q1 driving it out of conduction, thus applying -300 V to the control grid of the tetrode and shutting it off. Clamp 1 blocks the tetrode's conduction in $\leq$ 60 μs. A second clamp circuit (clamp 2) was installed on the output of A9 to shunt its signal to zero, thus phasing off the thyristors in S1. Clamp 2 blocks S1's conduction in $\leq$ 8.3 ms.

Start-Up

When starting up the power supply, two time delays are encountered. The first is a warm-up period for the tetrode series regulator, the second is for conditioning of the klystrons. With all CB's closed, an automatic start-up is initiated upon request for power from the remote klystron control. The warm-up period takes 52 s comprising:

- Contactor K3 closes energizing the filaments of the tetrode,
- The main contactor K1 closes 10 s later,
- The softstart clamp is removed 20 s later from the ac line regulator, and
- The softstart clamp is removed 13 s later from the constant tetrode voltage drop regulator and the voltage across the tube goes up to 1600 V.

Nine seconds after the above sequence a program for klystron conditioning begins which comprises a series of three pulse trains to the 14-bit digital-to-analog converter (DAC). These pulse trains are interspersed with 20 s blank periods.

- The first pulse train, lasting 45.9 s, counts the DAC to a reference equal to a 21 kV output of the power supply.
- The second pulse train, lasting 6.6 s, counts the DAC on up to a reference equal to a 24 kV output of the power supply.
- The third pulse train, lasting < 13.1 s, counts the DAC on up to a reference equal to the operating voltage requested by the klystrons.

Fast Shutdown

If a klystron sparks or if its focusing magnet malfunctions, the HV power must be removed as fast as practicable. Special circuits acomplish this as described below:

Klystron sparking: During normal operation, a klystron represents an 8 kΩ load. When it sparks to ground, the output voltage appears across the STDT which can support 28 kV for 20 μs (at lower voltages proportionally longer). This generates an output on the secondary winding of the STDT which via clamp 1 blocks the tetrode, thereby removing the HV output. The STDT pulse also initiates blocking of the thyristors of S_1, closing shorting switch K2 and opening contactor K1.

Klystron focusing magnet failure: In this case a remote "fast disable," pulse will block the tetrode and initiate a shutdown as described above. In addition, if the output voltage has not disappeared after an adjustable time delay, the triggered vacuum gap (TVG) will be ionized to short the dc source. This requires trigger pulses with a repetition rate of 1 KHz. When the TVG conducts the ~ 2 kJ stored in C_1 + C_2 would discharge within ~ 50 μs and the TVG would recover its blocking capability. The 8H filter choke limits the rate of rise of current to ~ 3.5 A/ms which cannot sustain conduction of the TVG. Therefore, the TVG is being triggered until after contactor K1 has opened.

Overcurrent: The sum of the load currents is monitored and compared to an adjustable reference. If the threshold is reached, the TVG is triggered.

Operational Tests

The two power supply's outputs were connected in parallel to a 4 kΩ 200 kW resistive load which was made from over a mile of #20 AWG nichrome wire. In order to test the fast shutdown feature the open contacts of an HV vacuum relay in series with a 1.5 kΩ resistor were connected in parallel with the 4 kΩ load resistance. The relay was energized when the power supply was at full power causing the load resistance to drop to 1.1 kΩ for testing the fast shutdown protection circuit.

Results of different tests are shown in twelve photographs. When viewing pictures A1 through A6 and B1 through B6, the circuit of Fig. 1 should be referred to.

1. A1 – Incoming 3-phase ac line phase-to-phase without FL1.
   B1 – Same as A1 but with FL1.

2. A2 – Output voltage, as the dc power supply is phased on, of rectifier bridges BR1 and BR2 without the filter FL2.
   B2 – Same as A2 but with FL2.

3. With the power supply operating at full power:
   A3 – Output voltage of the two rectifier bridges, BR1 and BR2.
   B3 – Voltage on the cathode of the tetrode.
   A4 – Voltage at the anode of the tetrode.

4. With a pulse from a pulse generator simulating the operation of the STDT, the responses can be seen of:
   B4 – Shorting switch K2 and the contactor K1.
   A5 – AC line regulator clamp.
   B5 – Tetrode clamp.

5. At full power, the load resistance was stepped down from 4 kΩ to 1.1 kΩ, and the resulting fast shutdown interlock operation is shown:
   A6 – Output of the STDT.
   B6 – Output of the tetrode (anode).

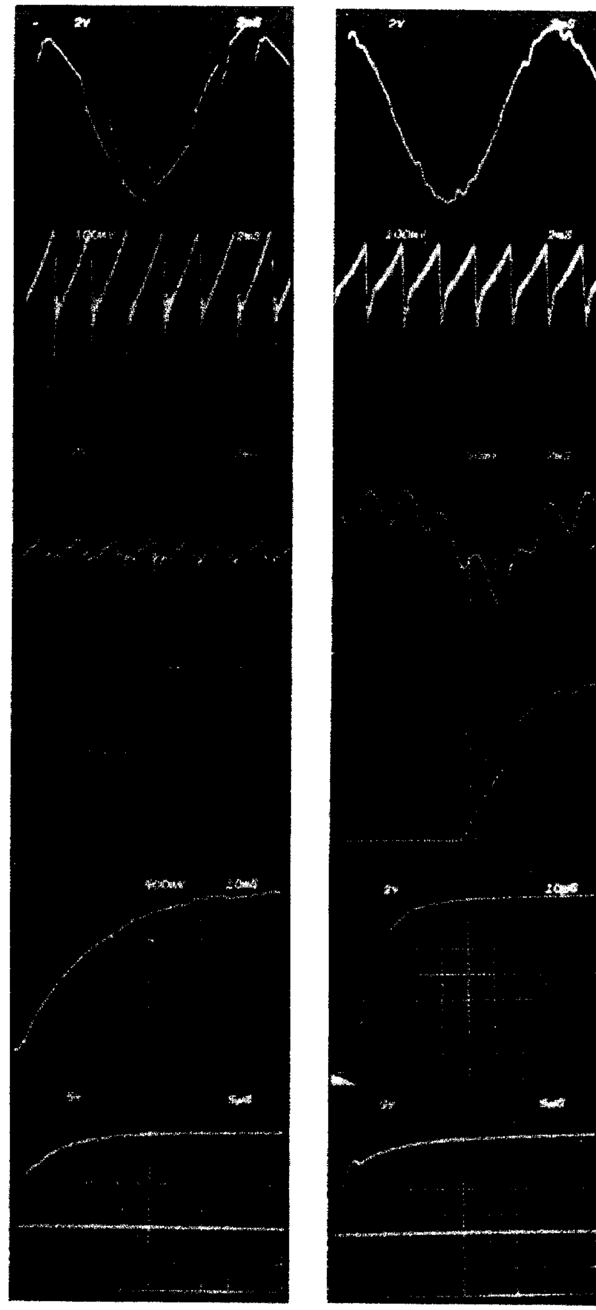

Fig. 3 Results of power supply test operations.

References

1. W. F. Praeg, "Overcurrent Protection for the TFTR Neutral Beam Sources During Spark Down," Proc. of the 8th Symposium on Engineering Problems of Fusion Research, San Francisco, Nov. 1979.