A SOLID STATE HIGH POWER AMPLIFIER FOR DRIVING THE SLC INJECTOR KLYSTRON*

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Abstract

The SLC injector klystron RF drive is now provided by a recently developed solid-state amplifier. The high gain of the amplifier permits the use of a fast low-power electronic phase shifter. Thus the SLC computer control system can be used to shift the phase of the high-power RF rapidly during the fill time of the injector accelerator section. These rapid phase shifts are used to introduce a phase-energy relationship in the accelerated electron pulse in conjunction with the operation of the injector bunch compressor. The amplifier, the method of controlling the RF phase, and the operational characteristics of the system are described.

Introduction

For the SLC (SLAC Linear Collider), electron and positron single-bunch beams at 50 GeV are to be produced by an upgraded SLAC linac. The linac is a traveling-wave RF accelerator operating at 2856 MHz (S-band). The SLC electron injector utilizes sub-harmonic bunching prior to S-band bunching to achieve a charge of over 8 nC in a single S-band bunch at relativistic energies.[1] In the injector accelerator section, after approximately 30 cm, all the bunched particles travel synchronously with the RF phase at $\beta = \beta_p = 1$ so that no additional bunching takes place. The beam is further accelerated to 1.2 GeV and injected into a damping ring (DR) to reduce the transverse emittance. Because the accelerating RF is sinusoidal, the energy spread of the beam in the linac increases with bunch length. On the other hand, for extremely short bunches, the energy spread increases due to the effect of longitudinal wakefields generated in the accelerating sections.

In order to optimize the bunch length at the injector, the path-length of the bunch is varied as a function of energy by passing the beam through a bunch compressor consisting of four dipole magnets.[2] If the phase and energy of the particles in the bunch are correlated, the compressor can be used to adjust the bunch length. The desired correlation can be accomplished

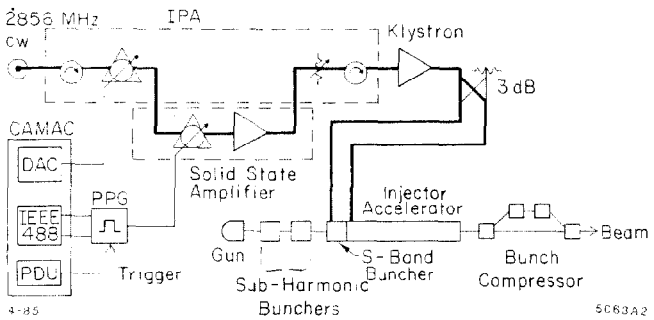

Fig. 1. SLC Injector RF block diagram. IPA—Isolator, Phase shifter, Attenuator. PDU—Programmable Delay Unit. PPG—Programmable Pulse Generator.

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by shifting the phase of the injector klystron in a time that is short compared to the fill-time of the accelerating section (0.8 μsec). The timing of the phase shift must then be adjusted so that an electron bunch passing through the 3 m section sees the phase shift somewhere between 30 cm and the end of the section. If the RF phase is shifted so that in the latter part of the acceleration the bunch is advanced in phase with respect to the crest of the RF, then at the compressor the lead particles will have less energy and consequently take a longer path through the compressor than the particles in the tail of the bunch. By adjusting the strength of the compressor magnets and/or the timing and magnitude of the phase shift in the injector RF, the bunch length can be adjusted for a σ_z in the range of 1 to 4 mm.

A fast phase shifter for the high-power RF output of the injector klystron does not exist. However, the bandwidth of the klystron is quite sufficient if the phase of the RF drive is shifted instead (Fig. 1).

Amplifier System Description

The new amplifier system consists of a four-stage pulsed amplifier and low-level microwave signal conditioning circuits (see Fig. 2).

The amplifier is built around 60 Watt S-band transistors developed by Microwave Semiconductor (MSC) and Acrian. These silicon bipolar transistors have approximately 6 dB of gain.

The 60 W transistors are paired into a 120 W module using 3 dB microstrip hybrids. By combining the power of four 120 W modules, 450 W are achieved. The amplifier output goes through a variable attenuator and isolator with a combined minimum loss of 1.5 dB before reaching the klystron. This means a maximum drive of 320 W is available at the klystron. The combining is done by a four-way stripline hybrid system. The same four-way system is used in a reciprocal fashion to split the drive to each module. A fifth 120 W module is needed to drive the output stage.

This 120 W module is fed by a 32 W pulsed power amplifier. It is a two-stage 12 dB gain module using lower power versions of the 60 W transistor. The 32 W amplifier requires 2 W of drive which is supplied by a commercially available high-gain FET amplifier.

The low-level signal conditioning circuits consist of linear 0 to 180 degree phase shifter, PIN diode pulse modulator, electronic variable attenuator, and $\pm\pi/2$ phase shifter (PSK).

Pulsed Power Transistors

The high-power transistors are common base internally grounded with collector efficiency of 35%. Internal matching and bond wires to the die limit the bandwidth to 200 MHz. Maximum pulse width of 100 μs and 10% duty cycle are limited by the device's thermal time constant. Operation above these limits decreases the lifespan. Accelerated life tests being

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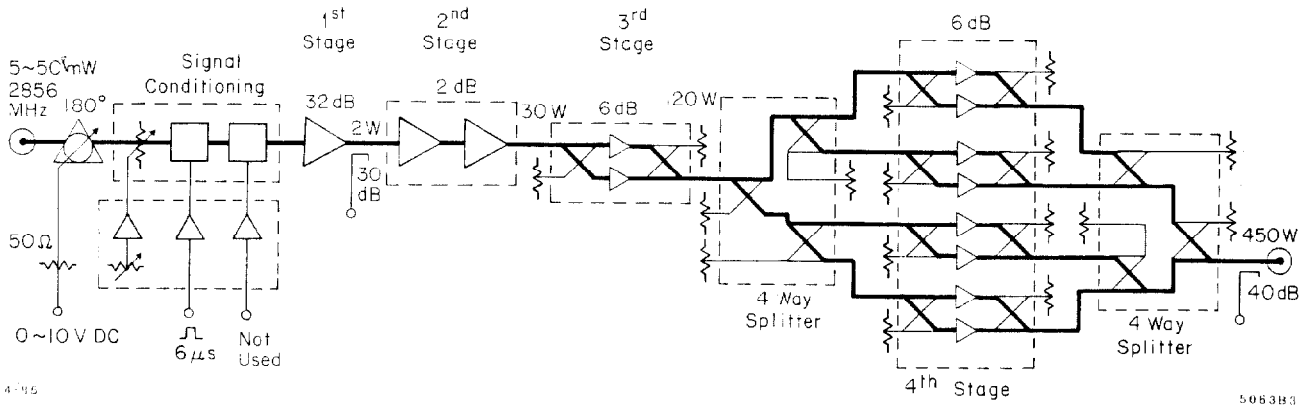

Fig. 2. S-band solid state amplifier block diagram.

done at MSC over the past five years suggest a mean-time-to-failure (MTTF) of well over ten years.[3] These tests are not conclusive yet.

Pulsed operation never lets the temperature of the transistor junctions stabilize. The collector region carries the bulk of the current and sees the greatest effect of this temperature rise. It is believed that the collector N^--layer resistivity changes due to the temperature change.[4] This varying series resistance together with the collector-base capacitance forms an RC network which results in an exponential phase change of approximately 6° during a 5 μs pulse. Increasing input drive or collector voltage in turn increases the rate of thermal rise and can be correlated to an increase in phase change during the pulse.

Collector base capacitance varies with collector voltage. The phase dependence to collector voltage is approximately 1.5° per volt. Therefore, voltage droop must be kept to a minimum or it will compound the problem of phase change during the pulse. This is done by providing enough energy storage capacitors necessary for flat pulse top. We have found 15 μfd locally for each transistor is sufficient. A printed low-pass filter on the circuit board isolates the RF from the power supply. By providing just enough capacitance protects the transistors from continuous wave (cw) drive or wide pulse widths. The current limiting series voltage regulator for each module start limiting at 60 μs pulse length. This is 60% of the recommended maximum of 100 μs. The emitter base junction can withstand cw drive. The second protection mechanism is the PIN diode modulator. It turns the RF drive off in its default position with no video input.

Amplifier Modules

The 120 W module major components are two 60 W transistors and two 3 dB 90° branch-line couplers. Matching circuits and couplers are microstrip circuits printed on teflon fiberglass. The couplers split the input and combine the output power. The isolated ports of the couplers are terminated externally to the module. This permits monitoring of circuit performance during tune-up.

During tune-up, input reflections and power emitted from isolated ports are minimized while output power is maximized. Tuning is accomplished by incorporating variable capacitors on the input and output circuit of each transistor. Initially collector voltage and input power are set to one-half the final value. This minimizes transistor damage due to circuit defects and mistuning. Fine tuning is repeated at 35 V. Final tuning and voltage setting is based upon power output, pulse shape, minimal phase change during the pulse (Fig. 3), and relative phase length of the module not to exceed ±10° relative to a standard module. Final collector voltage varies between modules from 40 V to 44 V. It has been found that the relative phase length between modules can be kept to within 5° with little effort in tuning. The serial number and voltage is recorded for each module. Each module has its own voltage regulator with current limiting. When put together as a system, each module's VCC supply is adjusted to the recorded value. No tuning is required for the assembled system.

The four-way splitter/combiner consists of three 3 dB branch-line couplers. The arrangement of input and output ports is such that it can be used for splitting and combining power. Termination of isolated ports is done externally to the stripline circuit where terminations for the proper power level can be selected. The stripline circuit itself can handle up to 4 kW of pulse power without noticeable breakdown.

The interconnecting cables between the splitter/combiner and 120 W modules are kept to within ±5° relative phase length. This is accomplished by cutting cable the same length and bending to fit its position. Each cable is then tested on a network analyzer. This simple method produces cables to within 3° of one another.

Assuming a worst case path length error in the combining of modules of ±15°, the power output loss would be 0.3 dB (3.4%). The combining loss noted in the three amplifiers built is 0.25 to 0.3 dB. This loss is accounted for by conductor loss in the combiners and cables.

The second stage 32 W amplifier is a product of the same pulsed transistor technology. It uses a 6 W and 35 W transistor in series, each with 6 dB gain. These lower power versions of the 60 W transistor exhibit the same phase change during the pulse, but to a lesser degree. The phase change for the module with two transistors in series is approximately 6°.

The 32 dB gain FET amplifier has exhibited no phases change during the pulse. It is not known whether high-power pulsed MESFET transistor would, but in this case the FET amplifier is Class A. Being Class A means it always has bias current flowing providing DC heating.

The total phase change during the 5 μs pulse is 18° for the entire system (Fig. 3d). Compensating for the phase change

has been demonstrated in the lab and will be implemented later on. It entails a pulse into an RC circuit. A variable resistor adjusts the exponential rise time of the network. This exponential voltage drives the control input of the electronic phase shifter and cancels the transistors phase change. This technique removes all of phase change after the first μs. The initial phase change is caused by the voltage drop of the power supply circuit when the transistors turn on.

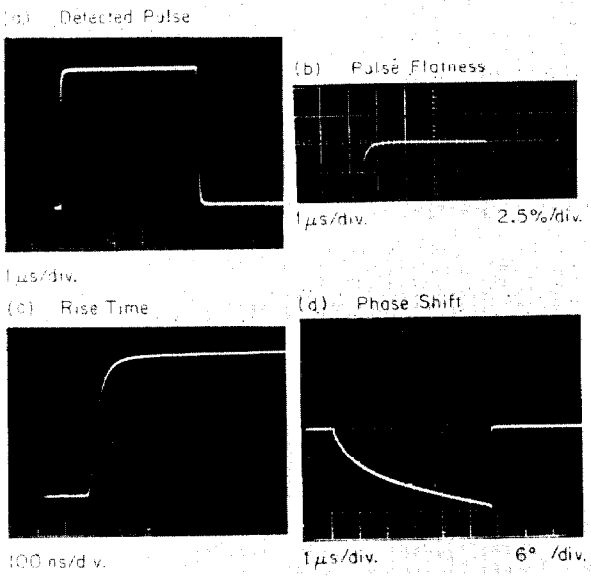

Fig. 3. RF pulse characteristics. 3d) shows exponential phase change of high-power pulsed transistors.

Low-level Signal Conditioning

Low-level signal conditioning circuits consist of two SLAC stripline circuit boards. One of these serves three functions. The cw RF input is pulsed by a PIN diode modulator. Pulse width and timing is externally supplied by a NIM logic pulse. Amplifier saturation is controlled from the front panel by an electronic variable attenuator. The PSK is not used in this application.

The second stripline circuit board contains the linear electronic phase shifter.[5] The phase shift is produced by voltage-controlled varactor diodes. The circuit provides a nearly linear 0 to 180° phase shift for a 0 to 10 V input. The response time is less than 20 ns.

To produce the desired phase-energy correlation in the injector bunched electrons, a step voltage must be used to modulate the RF phase of the amplifier (Fig. 4). The required step is generated by a commercial programmable pulse generator (PPG). The amplitude of the step is set by the SLC computer control program through an IEEE interface bus, while the step is timed independently using a programmable delay unit (PDU). The PDU is also used to select which of the RF accelerating pulses will be modulated by the step. All of the computer controls are accessible to the operator through standard SLC touch panels.

Conclusion

As of this writing, 4000 hours have been logged on a prototype installed September 1984, and 2000 hours on the present versions installed February 1985. The system has performed successfully with no degradation in performance.

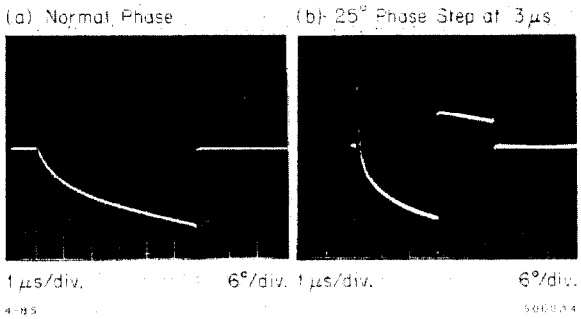

Fig. 4. a) Typical phase versus time. b) Example of phase step of 25° 3 μs into pulse.

The suitability of this amplifier as a general drive module for SLAC klystrons is presently being evaluated. Some SLAC klystrons require drive power up to 1 kW. Higher power can easily be provided by combining more modules, but efficiency of the combining network becomes of greater concern. Traveling-wave couplers allow combining of any number of modules, whereas 3 dB hybrids are restricted to binary configurations of 2, 4, 8..., etc. Combining more than four modules, the traveling-wave couplers have better efficiency. Also, both MSC and Acrian are developing higher power transistors of 100 W or more. This would nearly double the power of the solid state amplifier, making it even more competitive with the existing sub-booster klystron system.

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