THE BASIC TOOL: THE STARBURST J-11 HIGH SPEED FRONT-END PROCESSOR

F.H. Worm and D.V. Klotz
C.E.S. Creative Electronic Systems S.A.
Petit-Lancy, Switzerland

Summary :

Extending the on-board capacities :
- Memory
- Processing speed
- Data-acquisition speed

Extending the acquisition applications :
- The system Crate Interface
- The ADC interface
- The ECL bus interface

Extending the host computer interfaces :
- The ETHERNET interface

Extending the onboard memory capacity

With the possibilities of FORTRAN 77 written applications running under RSX-11S with micro Power PASCAL applications it became evident that more and more real-time tasks were being handled at the Starburst level and that the original memory capacity of 128 Kbytes would have to grow.
Therefore special SO format 8 Kbyte chips have been used with 2 chips mounted on a small PCboard which is pin-compatible with the 8 Kbyte RAMs (6764) for EPROMs. This provides 256 Kbytes of 120 ns access time on-board cache memory.
Another advantage of this solution is that RSX-11M can be run without any memory extension card on the Q-bus, thus reducing the space required by the system and boosting the performance by a significant factor (more than 3) as the full memory is now accessed as cache memory and does not require relatively slow Q-bus accesses.
For those applications requiring even more capacity an on-board memory of 512 Kbytes has been developped, using static RAMs.
Another improvement currently under test is the extension of the CAMAC porting to the full on-board memory and not only to the lower 128 Kbytes as it is at present. This will allow very efficient down-line loading of application programs without the need for any on-board memory shuffler.

Extending the system's overall speed.

The latest J11 chips are now running at 15MHz which means that when using 120us memory the overall speed is nearly doubled compared with the 8 MHz-equipped Starburst.

Increasing the CAMAC data acquisition rates.

CAMAC access to the J11 is memory mapped and is usually handled by programmed transfer (MOV instructions).
The average memory transfer time between a CAMAC module and a memory position is between 2.5 microseconds and 3.7 microseconds according to the type of MOV used. (2.5 is register transfer, 3.7 is indirect memory with auto-increment).
The CAMAC overrun processor allows a gain of up to 600 us, but for more significant improvements another system was needed.
A true CAMAC intelligent coprossessor card (the CAMAC BOOSTER CB 2182) has been designed to manipulate data blocks at the maximum CAMAC bus speed of 1MHz.
It features a comprehensive set of CAMAC commands to select which type of block transfer is needed (Qstop, Qscan, Qrepeat. LAM stop.) and to select the associated parameters, (word connt, direction etc.) The most commonly used transfer modes described in "EUR 6100 Block Transfer Modes in CAMAC Systems" are supported. The CB2182 features a direct access to the ACC 2180 memory via a private port which means that true direct memory access to any area within the onboard memory is realised at 1.2 us per word
Another advantage is that the J11 is not stopped during the transfer, thus allowing the CPU to process other data while the CB 2182 is active.

Increasing the Floating Point performance

The J11 CPU already comes with a microcoded floating Point instruction set which delivers an excellent performance, surpassing all the LSI-11 based machines and approaching the performance of a VAX 780.
The performance is more than 10 times that of a Falcon, and equals the FPF-11 performance.
For example a spectrum-analysis program written in FORTRAN-77 performed a complete qualitative and quantitative analysis of a 4096-channel spectrum (requiring intensive floating-point calculation) in less than 3 minutes compared with 24 minutes on a PDP-11/34.

However for floating point intensive applications such as transient analysis, high speed signal averaging, image reconstruction, etc., a significant improvement factor was needed.
No optimal solution was found, Floating Point Array Processors being much too expensive and the existing Floating Point Processor chips compromising the software compatibility for high level programming.
Then we had the chance to receive a DEC chip especially designed for the J11 and the VAX chip - a warm floating point asynchronous co-processor.
This chip with its ancillary logic may be mounted as an option on the CB2182, or may be used alone on a piggy-back board (FPB 2185).
It is a fully asynchromous coprocessor communicating with the J11 "attached Processor" pin and it boosts the floating point speed by a factor of between 3 and 8; (5 on average)
This proved to be an excellent solution as a replacement of very expensive floating point extensions by arrays of ACC 2180s equipped with FPB 218s.

Extending the Acquisition Applications.

The system Crate Interface

Being an Auxiliary Controller or a Stand-Alone Controller, the ACC 2180 is only able to control one CAMAC Crate.

0018-9499/85/1000-1923$01.00© 1985 IEEE

For control of experiments requiring more than one Crate a Branch Driver Extension was required.
The most popular system in operation being the "System Crate Concept", a system Crate Interface was designed.
Use in conjunction with an ACC 2180 an MX-CTR Executive Controller and a BC Branch Coupler, it allows one or more CAMAC Branches to be controlled from a single ACC 2180-SCI 2280 Combination.
The SCI 2280 is a single width CAMAC module connected to the ACC 2180 Q-bus via its Q22 or to another Q-bus machine, and emulating the programmed transfer and Interrupt Controller of the original system Crate.
It drives System Crate branches at about 3 microseconds/word and requires no modification to existing software. Other ACC 2180s used as in-crate processor at lower leverls and the ACC 2180 driving the branch can be lused as front-end branch processors whire data correlation is handled.

Interfacing with ADCS/TDCS.

The interface with the ADCs may be done directly via the CAMAC interface if the ADC is equiped with a CAMAC read-out system; or through an interface module if either the ADC has no CAMAC interface or is equipped with a private read-out bus allowing a higher bandwith.

Interfacing spectroscopy ADC

The Interface module is a dual port memory (HM 2161) One port is the CAMAC port used to retrive data, the other port is a front-panel port which is used to enter data coming from the ADCs or TDCs.
The memory is 64 Kwords deep, 24 bits wide and has a bandwith of 1MHz both in histogramming and list modes. It is a single-width module. The adaptation to the most popular ADCs currently on the marked is done via control logic implemented by PALs.
It offers the advantage of releasing the J11 CPU from the cumbersome histogramming computations, and creates a data base easily accessible from the J11 CPU without consuming on-board memory.
Several ADCs can be interfaced with one Histogramming Memory through a multiplexer system and both Spectroscopy ADCs of Fast ADCs may be interfaced.
Memories can be used either in LIST or HISTOGRAMMING mode and several memories can be cascaded to provide up to 1MWord of data memory.
A memory router designed by GSI Darmstadt in collaboration with CES can be added to the system to allow recording of several runs in the same memory, the spectrum being shifted each time by an externally applied shift count.

Interfacing ADCs equipped with an ECL port.

The interface is equipped with an additional unit containing an ECL high speed memory working as a buffer between the ADC and the HM 2161 memory.

Extending the host computer interconnection facilities

Up to now, 2 interfaces are available :

CAMAC interface
RS232C interface

A ETHERNET interface network has been added using the DEC DEQNA card allowing a STARBURST workstation equipped with disks to be connected to a VAX host computer or to another STARBURST work-stations.
The bandwith of the ETHERNET link is not as high as the CAMAC link handwith but the processing power of the STARBURST is more than adequate to solve all time critical computations before transfer to the host computer, and it creates a software transparency which makes connections much easier (transparent logins, direct file transfers, etc.).
An EPROM resident version of the ETHERNET driver should complement the disk based ETHERNET driver extending the connections from disk equipped work-stations to single slot front-end processors.