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COMPUTER CONTROL OF RF AT SLAC*

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Introduction

The Stanford Linear Accelerator is presently being upgraded for the SLAC Linear Collider project. The energy is to be increased from approximately 31 GeV to 50 GeV. Two electron beams and one positron beam are to be accelerated with high demands on the quality of the beams. The beam specifications are shown below in Table 1:

Table 1. Some SLC Specifications for the Linac

Energy, E	51.5 GeV
$\Delta E/E$	$\pm 0.5\%$
Particles per bunch	5×10^{10}
Bunch length	1 mm
Beam emittance	3×10^{-10} rad meter
Repetition rate	180 Hz

To meet these specifications, all parameters influencing the beams have to be under tight control and continuous surveillance. This task is accomplished by a new computer system implemented at SLAC which has, among many other functions, control over RF accelerating fields.

Historically, the 3 km long SLAC linear accelerator provides RF accelerating fields at 2856 MHz using about 245 high-power klystron stations.[1] The stations are grouped into thirty sectors with eight klystrons each, plus an injection sector. The distribution of the RF signal and the typical layout in the first sectors is indicated in Fig. 1. A continuous wave (cw) RF signal at 476 MHz is distributed to the sectors along the linac via a Main Drive Line (MDL). At each sector level a frequency multiplier increases the frequency to 2856 MHz. A pulsed sub-booster klystron amplifies the RF to 60 kW which provides a maximum of 4 kW drive signal at each high-power klystron station. In the past an assortment of 20 MW to 35 MW klystrons were used in this position capable of operating with a 2.5 μs pulse width at a maximum repetition rate of 360 Hz. For the SLC operation of the linac, these klystrons are presently being replaced with tubes capable of producing 50 MW power for 5 μs with 180 Hz rep rate. The pulse length was increased to 5 μs in order to utilize the energy compression of the SLAC Energy Doubler (SLED) system.[2] In this system RF energy is stored in two high Q cavities for 4.2 μs. The drive phase to the system is inverted by 180° at 0.8 μs before the end of the klystron pulse. This causes the stored energy in the SLED cavities to discharge and travel in addition to the

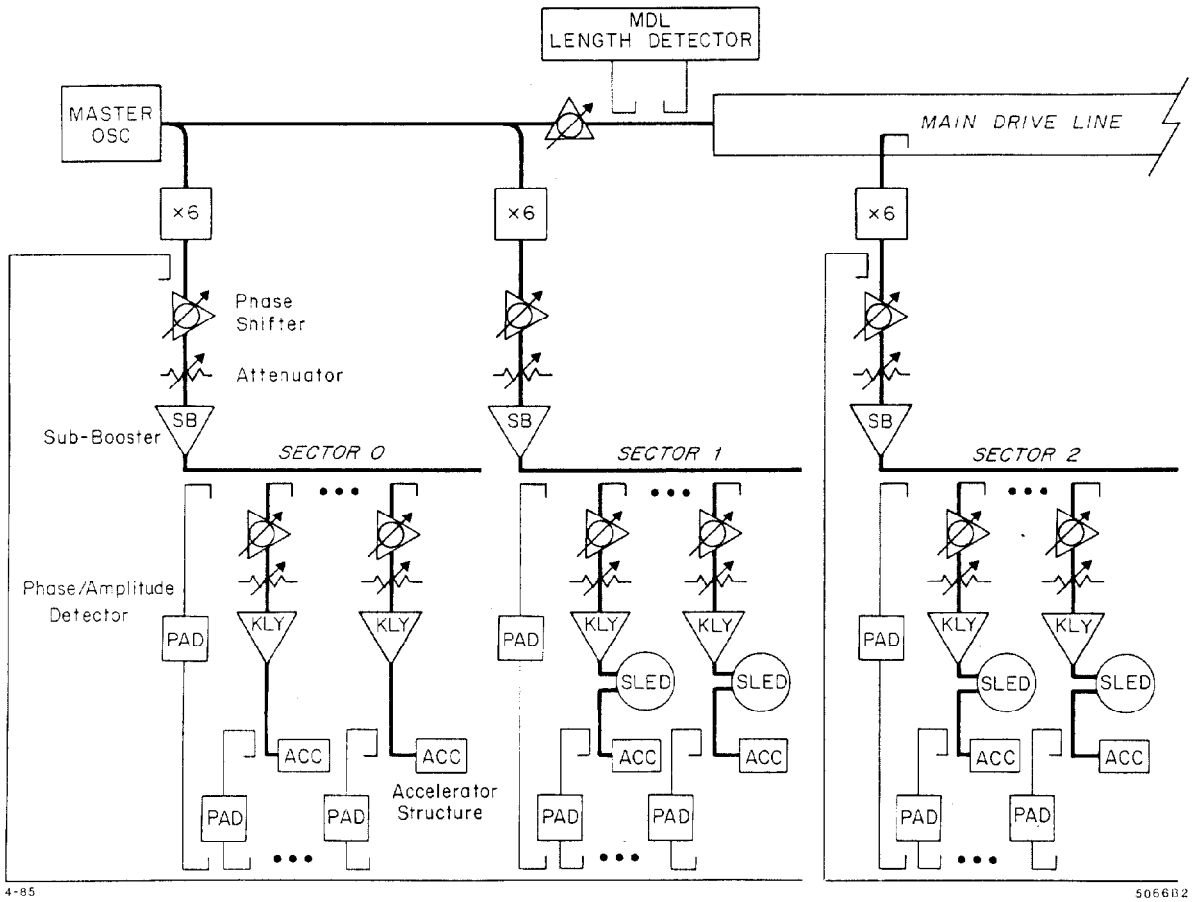

Fig. 1. RF system of linac Sector 0 to 2.

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klystron power towards the accelerating structure. The pulse at this point has the shape as shown in Fig. 2. The 0.8 μs long pulse with a peak power of 300 MW is filling the accelerator structures, four per station, each with a filling time of 0.8 μs. The three SLC beam bunches are then accelerated through the accelerator structure at the appropriate time.

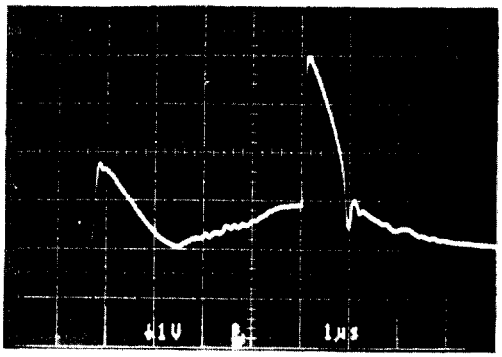

Fig. 2. Amplitude of SLED pulse.

In order to meet the high quality requirements of the SLC beams, the amplitude and phase of the accelerating RF fields have to be very stable from pulse to pulse. Table 2 shows the established jitter specification for Sectors 2–30. Sectors 0 and 1 are somewhat less critical since the beam emittance is improved in electron and positron damping rings after Sector 1.

Table 2. Maximum Jitter Specification

Sector	Phase Jitter (degrees)	Amplitude Jitter (per cent)
2	0.1	0.1
3	0.2	0.2
4-5	0.3	0.4
6-30	0.5	0.5

The SLAC RF system was originally built with emphasis on stability. Much attention was given to stabilizing all drive lines and waveguides, as well as the accelerator sections themselves, with temperature controlled water. Many klystron parameters are regulated. So, with only minor improvements, the SLC requirements for short-term stabilities can be met by a well-behaved station. However, detection of misbehaving stations and their diagnostics was considered essential. Also, long-term stability should be measured to detect environmental influences or drifts.

A computer controlled phase and amplitude detection system (PAD) was developed which would simultaneously measure magnitude and phase of the RF pulse at each high power station and each sub-booster station (Fig. 1). For the phase measurement a stable reference is required. Phase reference lines were developed operating in conjunction with the MDL, whose electrical length is measured.

To allow computer control of all the RF systems a variety of RF control elements were developed such as phase shifters and attenuators operating at power levels from milliwatts to kilowatts. In some cases fast-acting low-power control elements are used in conjunction with a newly developed transistor amplifier capable of producing 450 W of pulsed power at S-band. This amplifier provides the drive signal to high-power klystrons and is considered a candidate for replacement of the sub-booster klystron. In the following report, each of these systems or components are described in greater detail. Eventually a rough overview of the computer architecture will be presented. The operation of the system will be described using interesting linearization procedures.

Phase and Amplitude Detector

The phase and amplitude detector has the following functions: provide a measurement of amplitude and phase of microwave pulses in the watt to kilowatt peak power range at 2856 MHz with pulse widths of 0.1 to 5 μs; produce video signals of the pulse measurement; take a sample of amplitude and phase at a computer-controlled sampling time and digitize these values; provide instrument control and calibration functions.

Physically, the instrument consists of two separate units (see Fig. 3). An RF head[3] contains the microwave printed circuit, video processing electronics and digitizing electronics. The controlling microprocessor is contained in a CAMAC module, the so-called Parallel Input/Output Processor (PIOP).[4]

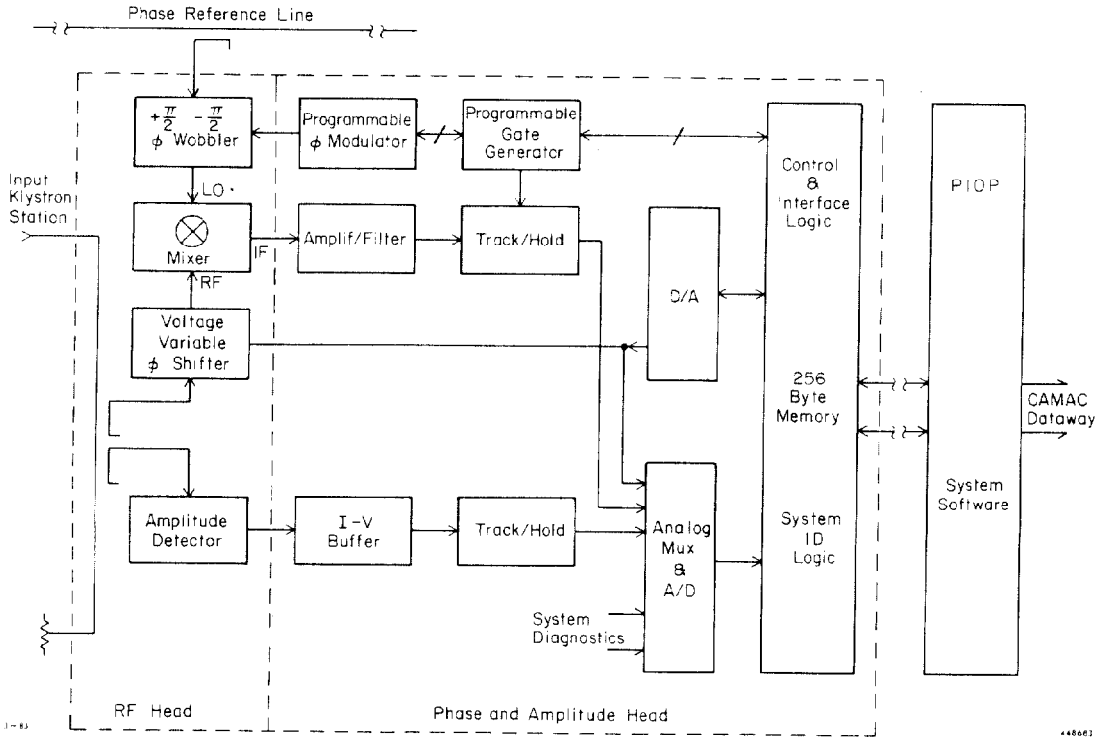

Fig. 3. Phase and amplitude detector system block diagram.

A rough description of the phase/amplitude detector follows. The amplitude detector is of a linear detector design where a diode rectifies the peak of the RF voltage. Its voltage linearity over a 20 dB range is ±5% and it has excellent long-term stability. The phase detector uses a mixer as a nulling detector with a ±90° phase wobbler in the phase reference line to resolve offsets. A quasi-linear electronic 180° phase shifter is used to null the mixer. The control voltage to this phase shifter contains the phase information over a 180° range when the mixer is properly nulled. The range is expanded to 360° by determining the sign of the slope at the zero crossing. All pulsed signals are sampled by sample-and-hold devices which are read into memory and then interrogated by the PIOP.

The phase is measured with a resolution of 0.1°. The absolute accuracy and linearity of the phase detector is limited by the linearity of the phase shifter and other factors to ±10°. Measurement algorithms and calibration routines to improve linearity to ±2° over a 360° range are described later.

Phase Reference Line

For accurate phase measurement a highly stable reference phase is required, which has to be available in 13 m intervals at every station along the length of the linac. To accommodate the frequent drop-out points, a reference line in an ultra-stable environment was chosen over the option of an electronically measured and controlled line. The foam dielectric cable with a low phase/temperature coefficient is concentrically enclosed by a water jacket with the water temperature controlled to 45 ± 0.1° C.

The line provides 10 mW cw reference signals at each station. To sustain this power level the reference line is divided into thirty sectors, each coincidental with the accelerator sectors and each driven through a stable amplifier after the frequency multiplication point of each sector. The 100 m long reference line sections were measured to be stable to < 1° in electrical length for ambient temperature changes of 30° C.

Main Drive Line Phase Length Measurement

With the above reference line arrangement, the MDL is part of the reference and has to be stable. The MDL consists of a temperature and expansion stabilized, pressurized, 3-1/8 inch rigid coaxial line operating at 476 MHz. Despite careful construction it displays phase changes with environmental changes mostly pressure related in the order of 60° at the accelerator frequency. A detector was built measuring the round-trip phase length of the line as shown in Fig. 4.[5] The forward signal is modulated at the end of the MDL and sent back. At the MDL input, this signal is coupled out and can be compared to a portion of the forward signal. Since the difference in signal level at this point is about 80 dB, a conventional phase measurement is no longer practical. However, a simple amplitude measurement with the help of filters and a synchronous detector can resolve the phase of the modulated signal in the combined vectors. A feedback loop then adjusts a phase shifter in the path of the modulated signal to bring the vector V_{mod} into quadrature with V_{ref} by minimizing the detected modulation (see the vector diagram in Fig. 4). V_{error} is caused by reflections along the MDL and has to be small or stable in phase. In this feedback loop the control voltage to the phase shifter again contains the phase length information for the MDL. This phase length information fed into the computer can make appropriately weighted adjustments to the sector phases, assuming the MDL changes phase length in a uniform fashion.

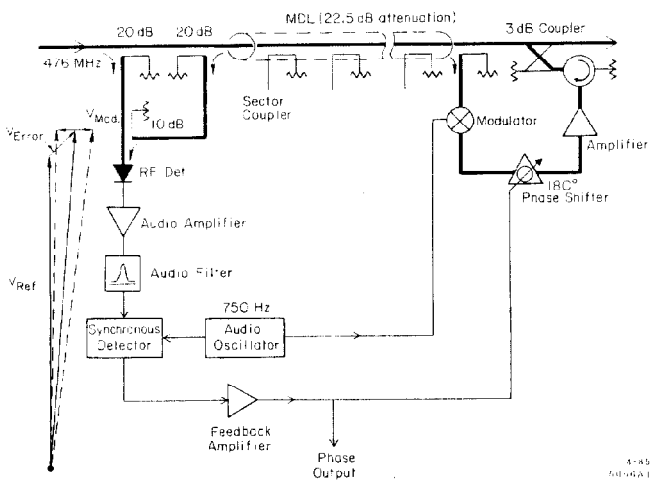

Fig. 4. MDL phase length measurement

A second method of phase comparison utilizes a fast sampling version of the phase/amplitude detector to measure phase of a very short (~ 100 ns) beam induced ringing in a single-cell cavity in the beam line. This measurement compares the reference line to our absolute phase standard, the beam.

High Power Variable Attenuator

One important control element in computer controlled RF is the variable attenuator. Low- and high-power versions of the same principal circuit are used, the high-power version operational at up to 2 kW of pulsed power at 2856 MHz. It controls the drive signal to the high-power klystrons.

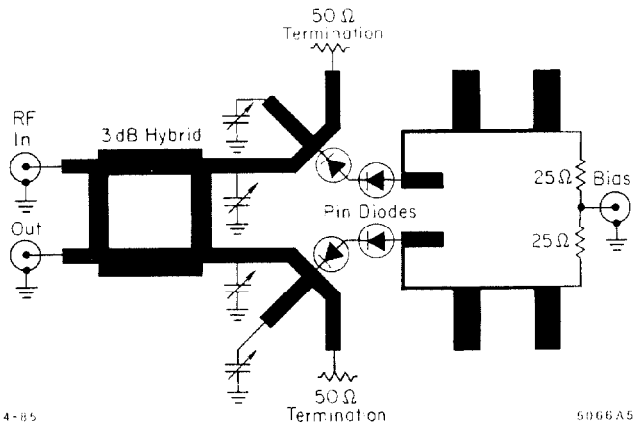

Fig. 5. Variable attenuator circuit (stripline).

The circuit uses high power PIN diodes[6] in a reflective mode which allows change of magnitude of reflection with only little variation in phase. An attenuation range of 35 dB can easily be optimized with a phase variation of < 10°. At the high power level, the PIN diodes do not display the ideal variable resistor behavior which leads to pulse distortion in regions of low bias current. Two effects occur with opposite results on the pulse shape. One is a depletion of charges in the transition region by the high RF currents when small bias currents are used. This effect can be minimized by using diodes with a long transition region and even adding additional diodes in series. The other effect is an actual rectification of the RF

signal producing a bias current which self-biases the PIN diodes. This effect is dealt with by not providing a path for this bias current to flow. So the high power attenuator has to be driven by a high impedance, low capacitance current source. The pulse distortion starts to be in the order of 0.5 dB at 10 dB of attenuation of a 5 μs pulse at 2 kW power level.

Computer Controlled Phase Shifters

Two types of phase shifters are in use. A low-power version usable below 40 mW provides 180° of continuous phase shift with a control voltage of 0-10 V (Fig. 6). A quasi-linear phase versus control voltage response is achieved by matching the nonlinear capacitance change of the varactor diodes to the nonlinearity of the phase of a variable reflection caused by the capacitance of the diodes[3,7] (Fig. 7).

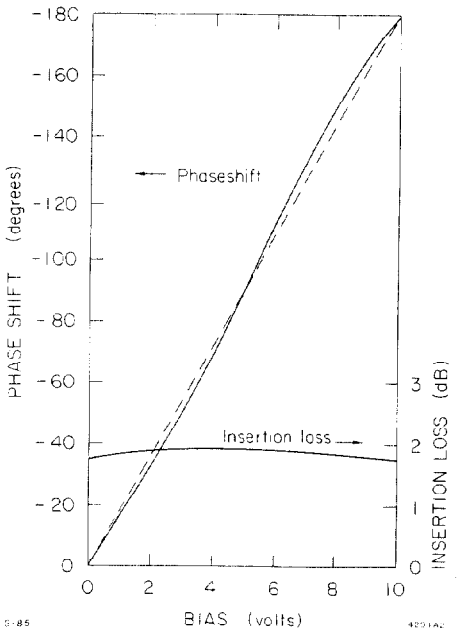

Fig. 6. Electronic phase shifter response.

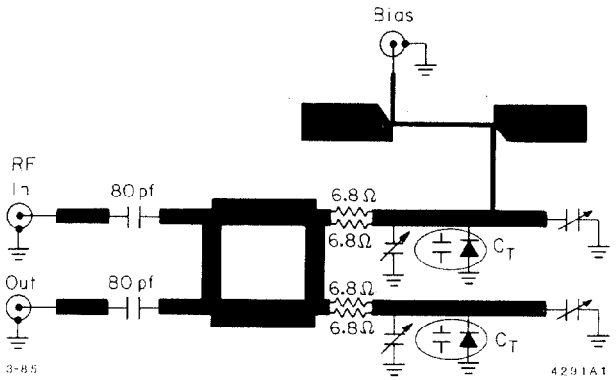

Fig. 7. Phase shifter circuit (stripline).

Variations in insertion loss over the control range have been minimized to ±0.1 db by use of lossy series elements.[7]

The phase shifter is being used in all positions where phase can be controlled at low power, including the phase/amplitude detector and applications at different frequencies, i.e., 476 MHz and 178 MHz. At the control input to the high-power klystrons at power levels of as much as 2 kW pulsed power, solid state phase shifters become impractical for continuously variable devices or cumbersome for switched devices using PIN diodes. For the SLC upgrade it was decided to continue to utilize the original mechanical phase shifters and control them from the computer via a stepping motor control. The phase shifters consist of circular waveguide sections with circularly polarized fields and a rotating half-wave length section producing the phase shift.[8,1] It can shift the phase by 720 electrical degrees for a full 360° mechanical rotation with a linear relationship between the two. The computer knows the position of this phase shifter by counting the steps of the stepping motor and referring to an optical reference point.

Solid State Power Amplifier[9]

To be able to use fast-acting low-power phase shifters or have independent control over one station, a solid-state power amplifier was developed. The amplifier provides the drive level required by high-power klystrons. Just recently bi-polar transistors have become available, providing as much as 60 W of output power at 2.7-3.1 GHz with a pulse width of 100 μs and 10% duty cycle.[10] Combining eight such transistors as output stage and providing the proper drive stages has resulted in a amplifier package with 450 W of output power at 2856 MHz. Some constant phase droop during the 5 μs pulse length of approximately 20° can be corrected by a feed-forward loop which applies an appropriate correction signal to a variable phase shifter at the input of the amplifier. The lifetime performance of the amplifiers is very promising and 4000 hours of operation have so far been accumulated without degradation or failure. Since the amplifier is a Class C device operating at a fixed power level, a high-power variable attenuator has to follow it if power level to the klystron is to be controlled.

SLC Computer Control System

The central part of the SLC control system is a VAX host computer (Fig. 8). The host computer is responsible for supporting operator interfaces, display generation, and allows time-based sampling programs to accumulate data for later analysis. The host computer communicates with a large number of distributed microprocessor clusters through a broad-band CATV based communication system.[11] Each microprocessor cluster is a multi-buss based Intel 8086/87 microcomputer which controls all devices in a geographical area (typically one sector) through a SLAC-serial CAMAC system. The microprocessor system is responsible for all peripheral interfacing and communicates with the host computer both through the SLC message service and through a shared data base. The microprocessor cluster receives beam pattern information from a dedicated channel on the CATV system, and broadcasts timing information to CAMAC modules prior to each pulse. Typical CAMAC peripherals include: DACs and ADCs for control of analog devices, beam position monitors, digital input/output modules, programmable delay units for generation of required triggers, and the Parallel Input/Output Processor (PIOP). The PIOP[4] is an Intel 8088 based intelligent controller which is used primarily for phase and amplitude measurement and klystron control. The interface for the klystron control is a special chassis called the Modulator/Klystron Support Unit (MKSU)[12,13]. It contains stepping motor drives for the control phase shifter, buffer circuits for the variable attenuator and a variety of circuitry concerned with timing, interlocks and klystron data acquisition.

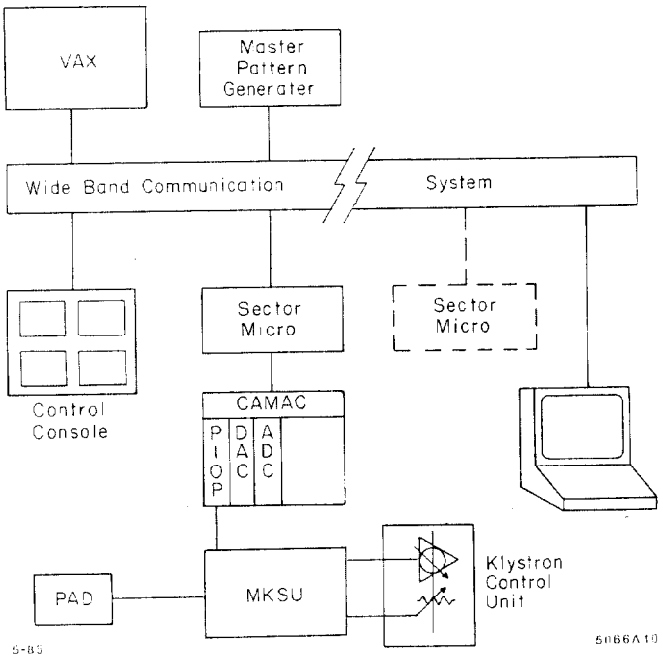

Fig. 8. SLC RF computer control system.

Operational Description

The program to operate the phase and amplitude detector is down-loaded into the PIOP from the local cluster micro. With the PIOP primed to a certain time slot the program finds the phase null through a simple search procedure and then calibrates the nulling detector wiggling the detector's phase shifter by $\pm 2°$ and wobbling the phase between 0 and 180° with the biphase wobbler. Detector gain, offset and sign of zero crossing are determined and the absolute zero calculated. Depending on the data acquisition mode the PIOPs program might then "freeze" the detector's phase shifters and depend on the linearity of the detector to calculate the klystron phase. The resultant phase information still contains the inherent nonlinearity of the phase shifter which is later removed by a system calibration procedure.

The PIOP will also (upon request from the host computer) measure a set of correlated data points for display in the control room or from portable consoles. These fast time plots (FTP) usually take the form of a set 64 sequential data points versus time within the pulse, resulting in a sampled waveform picture on the console (Fig. 9). Normal data acquisition is suspended

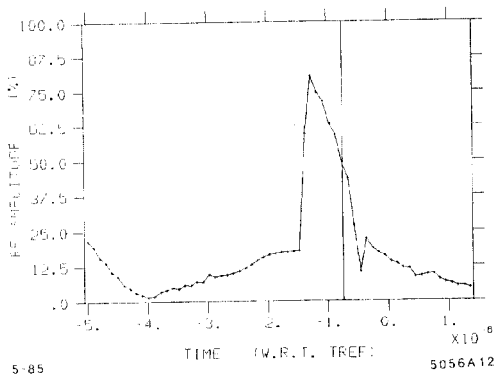

Fig. 9. Computer fast time plot of SLED pulse.

while the FTPs data is being acquired. The supported types of FTPs are:

- Phase or amplitude versus time (pulse shape)
- Phase or amplitude over 64 pulses (pulse to pulse jitter)
- Amplitude versus drive (saturation plot)
- Klystron voltage or current versus time or pulse to pulse.

To improve linearity of the phase detection, an off-line calibration routine located in the host computer can be run which measures the detected phase in comparison to the linear control phase shifter in the klystron drive. The program then uses the linear least squares method to calculate a polynomial which is stored in the data base in the cluster micro to be used for PAD data correction.

RF Control System Performance

The described system has been in operation in one-third of the SLAC linac for six months and has functioned very well. The availability of accurate long-term phase information has proven very valuable to the linac operation and fast fault detection is possible due to the jitter information on phase and amplitude and has led to improvements of the performance in individual stations.

Acknowledgements

The RF control system at SLAC is the result of the concerted effort of a large portion of the technical staff of the instrumentation and control group, the software group and the microwave engineering group. Keith Jobe has had the primary responsibility for the design and implementation of the software and computer interface and has made a major contribution to the successful operation of the system.

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