TIME-JITTER REDUCTION ON THE RF BUNCHER SIGNAL FOR THE LOS ALAMOS PROTON STORAGE RING (PSR)*

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Summary

The PSR at LAMPF will accumulate protons from the linear accelerator in both long- and short-bunch operational modes. Beam accumulation takes place for hundreds or thousands of turns. Ring buncher frequencies for these modes are 2.795 and 503.125 MHz, respectively. The bunching waveforms must be accurately correlated with the linac frequency standard so that the injected bunches fall into the ring rf buckets at precisely zero phase angle during accumulation. The PSR's rf wave also must have excellent phase stability. Long-term stability is assured by locking the PSR frequency reference to the linac's low-noise, temperature-stabilized crystal standard and by using delay-correction circuits in the transmission-line paths. However, the short-term stability of the rf reference signal is not as easily controlled because additive spurious signals can enter the long rf-signal transmission path (1-km linac-to-PSR), causing sideband energy increases very close to the carrier frequency. This increases time jitter. Also, some phase noise is spuriously developed by the signal-processing circuits providing frequency multiplication and division, the required processes for generating the necessary harmonic and subharmonic bunching frequencies at 503.125 and 2.795 MHz, respectively.

The measure of control pursued by the described circuit design will provide rf references with timing uncertainty much less than the expected uncertainty in the micropulse time of arrival at the ring, $\Delta T \approx \pm 80$ ps. For the short-bunch PSR mode where timing is much more critical than for the long-bunch mode, and where the bunching wave has a $\approx$2-ns period, a maximum uncertainty of ± 10 ps was chosen as the error budget for the low-level rf system.

This paper discusses the steps taken to develop the low-level rf reference signal with some measure of margin relative to this ±10-ps budget. Phase-locked loop stabilizers, narrow-band high rejection-rate filters, and low-noise multipliers/dividers provided the means to achieve the goal.

The multiplier described in this paper is part of a considerably larger system whose function is to generate several synchronizing signals for the PSR. Without examining the details, the larger sync system must, from a basic 201.25-MHz clock rate, generate phase-coherent, low-noise cw signals of 2.795 MHz for the LF buncher, 100.625 MHz for low-precision timing, and 16.77 MHz for the prebuncher in addition to the 503.125-MHz HF buncher described above. In very general terms, implementing these requirements involved dividing the 201.25-MHz clock rate by 72 to obtain 2.795 MHz and multiplying this rate by 6 to obtain 16.77 MHz using techniques very similar to those described in this paper.

General

The random variations in rf period can be characterized by the rf-wave's phase-noise spectrum. The rf-wave's phase-noise component and the timing uncertainty can be determined by establishing the sideband-to-carrier E_s/E_c level for a narrow-band FM/PM wave having a low modulation index m. The timing uncertainty Δt, needed to meet the short-term jitter goals, then can be estimated by relating the modulation index $m = \Delta f/f_m$ (containing the peak frequency shift Δf and modulation frequency f_m) to the peak phase variation $\Delta\phi$ and carrier frequency f_c.

The rf wave with added FM can be characterized by the time function

$$V(t) = E_c \sin [\omega_c t + \Delta\phi \sin \omega_m t] \quad , \tag{1}$$

where ω_c = carrier radian frequency $2\pi f_c$, ω_m = modulation radian frequency, and $\Delta\phi = \Delta f/f_m = m$ = peak phase deviation.

By application of several trigonometric identities and the Bessel series for sine and cosine terms with trignometric arguments, Eq. (1) can be transformed to a sideband time-function representation; that is,

$$\begin{aligned} V(t) = E_c \Big[& J_0(m) \sin \omega_c t + J_1(m) \sin (\omega_c + \omega_m)t \\ & - J_1(m) \sin (\omega_c - \omega_m)t + J_2(m) \sin (\omega_c + 2\omega_m)t \\ & + J_2(m) \sin \omega_c - 2\omega_m)t + J_3(m) \sin (\omega_c + 3\omega_m)t \\ & - J_3(m) \sin (\omega_c - 3\omega_m)t \ldots \Big] \quad , \end{aligned} \tag{2}$$

where the $J_n(m)$ terms are Bessel functions of the first kind of order n, with m = modulation index, the argument in all cases. Because $J_2(m)$ and higher order Bessel coefficients are negligible for $m \ll 1$, only the carrier term ω_c and the first sideband pair $(\omega_c \pm \omega_m)$ terms are significant. Also, the ratio $J_1(m)/J_0(m) = m/2$ for small m; therefore, the ratio of the sideband-to-carrier component can be shown to be $E_s/E_c = 20 \log (m/2)$ decibels; and the peak time shift Δt, caused by phase variations, then can be found as

$$\Delta t = \log^{-1}\left(\frac{\left.\frac{E_s}{E_c}\right|_{dB}}{20}\right) \times \frac{1}{\pi f_c} \quad \text{peak seconds} \quad . \tag{3}$$

Also, the sideband signal level relative to the carrier can be related to the peak time modulation by

$$\left.\frac{E_s}{E_c}\right|_{dB} = 20 \log (\pi f_c \Delta t) \quad \text{decibels} \quad . \tag{4}$$

For the circuit arrangement, Fig. 1, chosen for the low-level signal development, the timing and spectral parameters can be examined by Eqs. (3) and (4), using Eq. (3) to estimate peak timing jitter and Eq. (4) for determining the needed sideband-to-carrier level for meeting a specific timing requirement. Because the desired modulation frequency, or carrier offset value f_m is an important design parameter, f_m is chosen as $0.1/t_A = 1$ kHz, where t_A is the ring short-bunch accumulation time, 100 µs. Note that permitting f_m to be less than $1/t_A$, the change in the rf wave phase is small over the accumulation interval.

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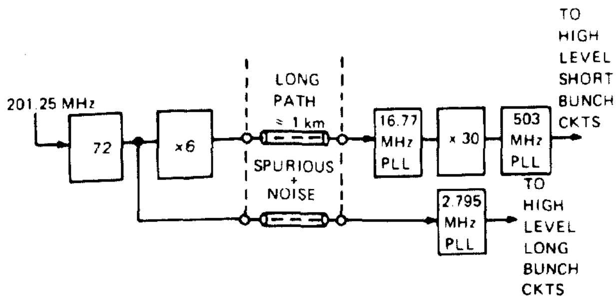

Fig. 1. Low-level rf generation.

Equations (3) and (4) estimate that there must be a sideband-to-carrier level of at least -36 dB at a 1-kHz offset to achieve the overall timing goal (±10 ps) of the low-level reference-signal development. A realistic margin beyond the goal is a factor of 5 (±2 ps), or a sideband-to-carrier ratio of -50 dB at the 1-kHz offset point.

The Multiplier

Frequency multiplication inevitably is accompanied by the generation of phase noise. Random phase noise on the fundamental rf wave generally becomes enhanced by an amount linearly proportional to the multiplication ratio N (for modulation indices <<1). Discrete FM spectral line amplitudes associated with the fundamental frequency will increase by 20 $\log_{10}$ N (dB) when multiplied by N.

Given a cw at a 16.77-MHz frequency, the required task is to generate its 30th harmonic, 503.125 MHz, free of close-in spurs and free of appreciable phase noise. Initially, one might consider predistorting the 16.77-MHz wave, using an impulse generator such as a step-recovery diode, and attempt to immediately select the 30th spectrum line. Such an approach presents formidable problems because, with an input spectral line spacing of 16.77 MHz, one must create a band-pass structure capable of passing 503.125 MHz while rejecting, by some substantial amount (say, 60 dB) all spectral lines >3% away from 503.125 MHz. Such a band-pass structure has serious design and stability-related problems.

Figure 2 shows an alternate and better approach, the one used for the PSR. The method shown is to factor the multiplication ratio, 30, into prime numbers, 5 X 3 X 2. Then, using ECL comparators with the reference point grounded, one can easily generate odd harmonics of the input wave. By placing the multiplication factors in descending order (5 X 3 X 2 rather than 2 X 3 X 5), filtering requirements become less stringent because it is easier to reject the fourth and sixth harmonics of 16.77 MHz as opposed to rejecting the fourth and sixth harmonics of 100.625 MHz.

Fortunately, the first two factors in the multiplication scheme (5 and 3) are odd, thus allowing us to take advantage of even-order harmonic suppression associated with a sine-to-square-wave conversion process. Unfortunately, ECL comparators toggling in the VHF range do not generate perfect square waves with zero rise/fall times and 50/50 symmetry. Nevertheless, the even-order harmonics in this process are suppressed ∿20 dB from the immediately adjacent odd-order harmonics, thus permitting satisfactory rejection of unwanted even-ordered spectral lines.

All lumped-constant filters following the first comparator are equivalent to band-pass functions and were implemented using Chebyshev 0.18-dB, seven-pole high- and low-pass configurations in cascade. This filter provides ∿60-dB attenuation one octave away from the filter's design cutoff frequency.

The final multiplier was a conventional high-level (+13 dBm) frequency doubler with good rejection (20 dB) of the fundamental and third harmonic.

Microstrip techniques using back-to-back quarter-wave lines were used for the filters following the X3 and X2 multipliers. At the junction of two back-to back quarter-wave transmission lines of high Z_0, a high-resistive impedance value is obtained at the center point, which lends itself toward good selectivity when a quarter-wave shorted stub of low Z_0 is placed across this point. The approximate lumped-circuit equivalent of this filter is a low L/C ratio parallel-tuned circuit driven by a constant-current source and terminated with an open circuit, giving excellent selectivity and good VSWR characteristics.

In summary, the multiplier accepts 16.77 MHz cw; generates the fifth harmonic (83.85 MHz); filters and amplifies this wave; triples its frequency to 251.55 MHz; and, after filtering and establishing the required signal amplitude, doubles this frequency to the final rf buncher frequency, 503.125 MHz.

The Loop

Phase-locked loops have several important applications in accelerator technology. One of the most important to the PSR is the active filtering of noisy rf cw signals. A noisy spectrum appearing as the reference input to a loop can be significantly "cleaned up" if the loop is configured for narrow-band closed-loop gain. Incoming phase-noise sidebands, whose distance from the carrier is greater than the closed-loop bandwidth, will be attenuated by an amount given by the closed-loop gain function. Equivalent "Qs" of several hundred thousand can be achieved with correspondingly low-percentage bandwidths using a phase-locked loop.

A high-quality, low-noise, voltage-controlled oscillator (VCO) with a narrow transfer function K_{VCO} (1660 Hz/V centered at 16.77 MHz) forms the PSR loop's core (Fig. 3). A standard level double-balanced mixer (+7 dBm) with an I-port response extending to zero frequency is the phase detector (ϕDET), which has the transfer function $K_{\phi DET}$ of 0.3 V/rad phase difference between the L and R ports. With a dc amplifier configured for 35-dB flat gain ($G_{dc} = \log^{-1} 35/20 = 56$), the OPEN-LOOP GAIN versus FREQUENCY, neglecting the filter transfer function F(S), may be written as

$$\frac{K_{VCO}\,K_{\phi DET}\,G_{dc}}{S} = \frac{1660 \times 2\pi \times 0.3 \times 56}{S} = \frac{175 \times 10^3}{S} .$$

This function's magnitude clearly decreases with increasing frequency at a rate of -20 dB/decade while its phase is constant at -90°. Determining that frequency f_u, at which the function's magnitude is unity,

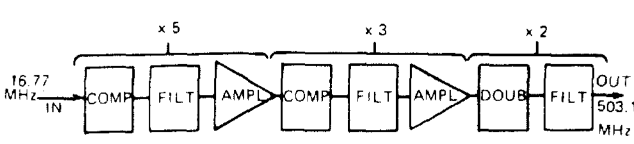

Fig. 2. X30 multiplier.

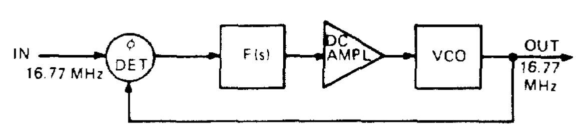

Fig. 3. Phase-locked loop.

is useful for examining stability and noise-reduction factors; we equate numerator to denominator and solve for f_u: Let $S = j\omega = j\,2\pi\,f_u$, $175 \times 10^3 = j\,2\pi\,f_u$, and $f_u = 28$ kHz.

If we were to close the loop without further shaping the open-loop gain, the closed-loop bandwidth would be 28 kHz, which is too wide for noise-reduction purposes. Consequently, a series of poles and zeros [F(S)] was implemented in a fashion necessary to guarantee unconditional closed-loop stability and to establish the closed-loop bandwidth at an acceptable value for effective filtering (100 Hz).

The loop-filter transfer function F(S), was implemented with the first pole (a down break) at 35 mHz, the first zero (an up break) at 10 Hz, and two subsequent poles beyond the closed-loop bandwidth at 400 Hz and 1.6 kHz. In this fashion, the open-loop gain crosses through unity at a nominal slope of -20 dB/decade, thus ensuring unconditional closed-loop stability while the ultimate gain change with frequency occurs at a relatively high rate, -60 dB/decade, thus ensuring good rejection for frequencies whose distance from the carrier is greater than the closed-loop bandwidth, 100 Hz.

The sideband rejection of the loop is best demonstrated by an example at the 16.77-MHz frequency. An incoming spectrum centered at 16.77 MHz with a 1-kHz FM modulation rate and 200-Hz peak-frequency deviation will have a sideband-to-carrier ratio of

$$\left.\frac{E_{SB}}{E_C}\right|_{IN} = 20 \log_{10} \frac{m}{2} \text{ decibels} \quad ;$$

where FM modulation index m = peak frequency deviation and Δf/modulating frequency f_m = 200 Hz/1 kHz = 0.2.

$$\left.\frac{E_{SB}}{E_C}\right|_{IN} = 20 \log_{10} \frac{0.2}{2} = -20 \text{ dB} \quad .$$

The loop rejection is ~28 dB at 1 kHz from the carrier; therefore, the output spectrum will have a sideband-to-carrier ratio of

$$\left.\frac{E_{SB}}{E_C}\right|_{OUT} = \left.\frac{E_{SB}}{E_C}\right|_{IN} - \text{SIDEBAND REJECTION}$$

$$= -20 \text{ dB} - 28 \text{ dB} = -48 \text{ dB},$$

a significant improvement.

Summarizing, the 16.77-MHz loop is configured for narrow-band closed-loop gain in a deliberate attempt to reject incoming noise whose frequency components are greater than the closed-loop bandwidth.

Using techniques quite similar to those described above for the 16.77-MHz loop, a second loop was used at the output of the X30 multiplier, centered at 503.125 MHz in an effort to reduce the noise generated by frequency multiplication. The noise reduction obtained was dramatic and is briefly discussed below in connection with the signal spectrograms. Figures 4, 5, and 6 are spectrograms of the HF buncher signal at 503.125 MHz and show the progressive reduction in spectral noise as each loop is added to the basic multiplier. Without any loops (Fig. 4), the close-in noise is ~41 dB below the carrier amplitude. With the 16.77-MHz loop added (Fig. 5), the noise drops to ~63 dB below the carrier amplitude. Finally, with the 503.125 MHz-loop added (Fig. 6), the noise is ~73 dB below the carrier amplitude. At this point, the spectral characteristics of the 503.125-MHz signal are very similar to the open-loop characteristics of the 503.125-MHz VCO, which characteristically has very low phase noise.

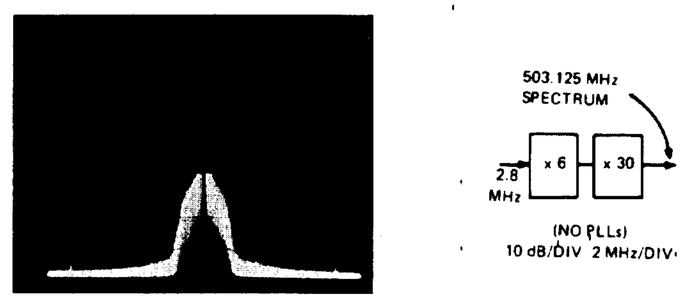

Fig. 4. The 503.125-MHz spectrogram (no PLLs).

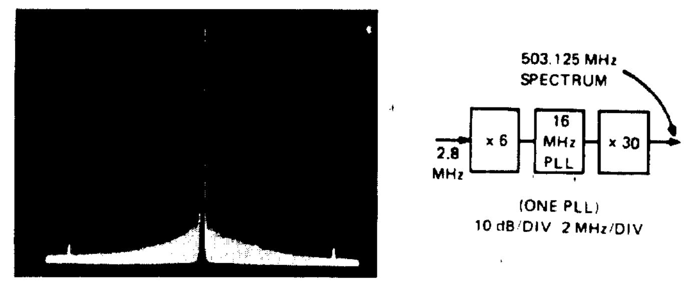

Fig. 5. The 503.125-MHz spectrogram (one PLL).

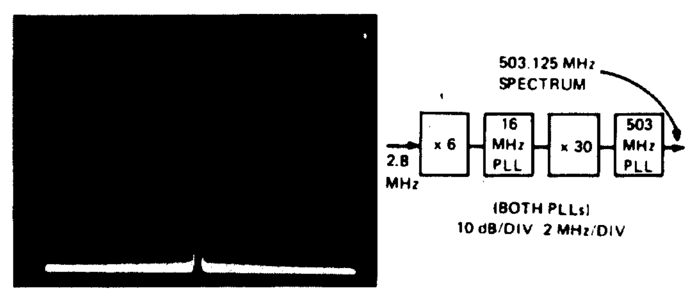

Fig. 6. The 503.125-MHz spectrogram (both PLLs).

Conclusions

Phase-locked loop stabilizers have been used in frequency-generating circuits to reduce phase noise. These circuits have reduced the time jitter for an rf reference signal for the PSR at LAMPF to less than ±2-ps peak jitter at a 503.125-MHz frequency, as evidenced by a sideband level 50 dB below the carrier level at a 1-kHz offset. Simple expressions have been introduced to predict the jitter performance of rf signal sources used in accelerator rf low-level systems. A method of frequency multiplication using fast comparators was outlined and has proven to be very useful for certain accelerator-related applications.

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