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REGULATOR TO CONTROL CURRENT SHARING AMONG PARALLEL-CONNECTED POWER TRANSISTORS*

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Summary

A current regulator is described that controls the peak current of a power transistor driving an inductive load, such as magnet coils. Presently, the current pulse has a 0.1- to 1-ms adjustable duration with duty cycle to 5%. Ultimately, the pulse length must be ∿7 ms with 50% duty cycle. The peak current nominally is 200 A, as set by a reference pulse. Several transistors, each controlled by an individual regulator, are connected in parallel to provide the total peak load current. The regulators compensate for differences between the power transistors and assure equal current sharing among the collectors. The regulator comprises an 8-bit multiplying digital-to-analog (D/A) converter that drives the base of the power transistor, an 8-bit up-down counter, an analog differencing circuit, and a comparator. For control purposes, a current-sensing resistor in the transistor's collector produces the second input to the differencing circuit. Regulation is accomplished over a collector current range of 200 ± 50 A per stage.

Introduction

In its short-bunch mode, the Proton Storage Ring at LAMPF will accumulate protons for 110 μs in six intense bunches spaced equally around the circumference. The bunched protons then will be extracted on a bunch-by-bunch basis over an ∿7 ms interval, repeating at 8.33-ms intervals. During the accumulation phase, and also as the bunches are extracted, changes in beam-loading are compensated by alteration of the bunching-cavity frequency. The bunching cavity tuning is accomplished by changing the permeability of ferrite material that fills a portion of an attached tuner element. The variation in permeability is achieved by rapidly changing a magnetic bias field applied to the ferrite, using a low-inductance magnet driven by a high-current modulator. Needed for tuning are magnetic field intensities of 1600 to 1850 ampere-turns, programmed throughout the cycle.

One candidate current driver for the tuner magnet is a grouping of parallel-connected Darlington transistors, each designed to contribute a portion of the current. In this circuit, each transistor is embodied in a feedback arrangement that regulates the current set by a program voltage, while feedback forces current sharing among the transistors. A circuit description is given in the following sections, and the laboratory test results are summarized.

General

Transistors frequently are used in a parallel connection to obtain more load power delivery capability. When the parallel connection is made, care is necessary to prevent differences in individual transistor characteristics from causing excessive dissipation in the device having the largest transconductance. Figure 1 shows a parallel connection in which each transistor has a different base-emitter voltage (V_{be}) versus collector-current (I_C) characteristic. For the conditions shown, transistor Q_1 will supply most of the load current because it has the largest

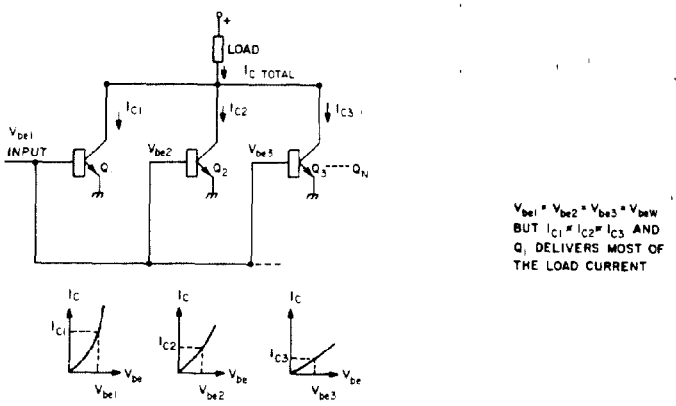

Fig. 1. Current sharing, no emitter feedback.

transconductance, $S = K(I_C/V_{be})$. Because the slope of the transconductance versus temperature function is positive for increasing junction temperature, Q_1 may end up supplying the total load current until it fails from dissipation beyond its capability.[1]

For a useful parallel connection, the current division among the parallel paths must be equalized and kept within device ratings. A possible approach is to match the individual transistors' I_C/V_{be} characteristics but this method is costly because of matched devices' low yields. Also, aging can result in mismatched devices after relatively short service time.

One alternative approach is to add resistance from the emitter terminal to the power-supply return terminal (Fig. 2).[2] In this approach, the I_C/V_{be} characteristics of an ensemble of transistors are examined for worst and best transconductance. The emitter resistor value, R_e, then is chosen from

$$R_e = \frac{V_{be1} - V_{be2}}{I_{C2} - I_{C1}}, \text{ ohms;}$$

where

I_{C1} = nominal collector current desired per transistor, within device rating;
I_{C2} = $(I_{C1})M$;
M = matching factor with magnitude greater than 1, that is, 1.1 = matching to 10%;
V_{be1} = worst transistor V_{be} at I_{C1} value;
V_{be2} = best transistor V_{be} at collector current $(I_{C1})M$.

By adding R_e in each parallel path, the collector currents equalize within the fractional part of M, making the voltage drop across the emitter resistor large compared to the V_{be} differences. However, this scheme's drawback is that large power dissipation takes place in the resistors, and large heat sinks are needed. The problem is compounded if the spread in transistor characteristics is wide, because R_e then will be large and additional transistors will be needed to make up for the resulting power loss.

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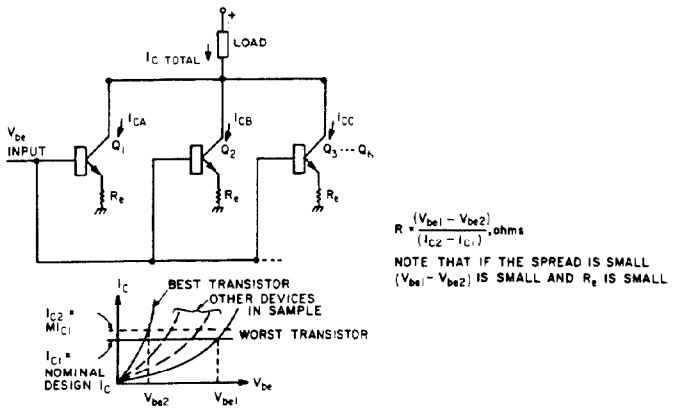

Fig. 2. Parallel transistors with emitter resistors.

In Fig. 3 another alternative is shown for paralleling the transistors so that current sharing and reduction in non-load dissipated power are achieved. Here, current sharing is achieved by adjusting individual input drive potentials (V_{be}) to the transistors. Each drive potential is set by measuring the collector current of a specific transistor in the parallel array and comparing the voltage measure of this current with the input drive signal E_{IN}. The returned amplified difference, d, is used to modulate the individual V_{be} voltages, so that each transistor delivers the same current to the common load.

The node potentials of Fig. 3 are expressed as

$$V_{be1} = E_{IN} X_1;\ X_1 = \text{numeric multiplier parameter.} \quad (1)$$

$$I_{C1} = K_4 V_{be1};\ K_4 = \text{transconductance constant.} \quad (2)$$

$$V_{I1} = K_o I_{C1};\ K_o = \text{transfer constant in ohms.} \quad (3)$$

$$V_{C1} = (E_{IN} - K_o I_{C1})\, G_1;\ \text{volts.} \quad (4)$$

$$X_1 = K_{X1} V_{C1};\ K_{X1} = \text{transfer constant in volts}^{-1}. \quad (5)$$

From these equations, assuming a simple relationship between collector current and emitter-base voltage for each transistor, the collector current is

$$I_{C1} = (K_4 K_{X1} E_{IN}^2 G_1)/(1 + K_o K_4 K_{X1} E_{IN} G_1) \quad , \quad (6)$$

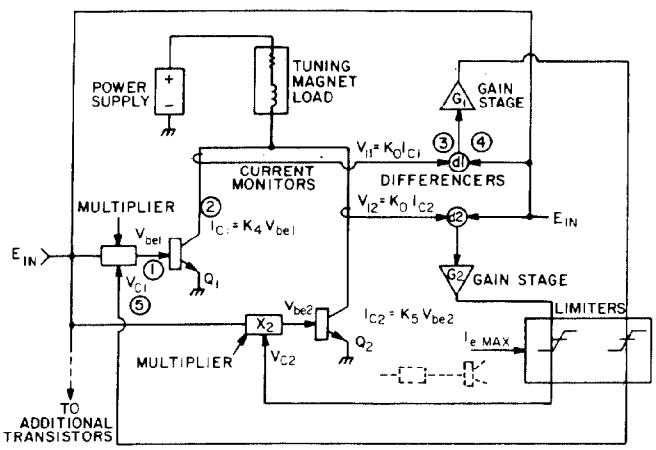

Fig. 3. Collector current equalizer using feedback.

and I_{C2} has a relationship of similar form. By letting G_1 be >>1, the term $K_o K_4 K_{X1} E_{IN} G_1$ can be >>1, and

$$I_{C1} = I_{C2} = \cdots = I_{CM} = E_{IN}/K_o. \quad (7)$$

Thus, the collector currents can be made proportional to the input signal E_{IN}, and equal to each other by feedback loops with large forward gains G_1, G_2, ..., G_n. An experimental circuit to demonstrate the process at current levels to 400-A peak is described below.

Current Regulator

Figure 4 is a circuit schematic of the current regulator. The input circuit is an 8-bit multiplying D/A converter that drives amplifier A1. The output from A1 is a voltage proportional to the product of the input pulse level and the digital number supplied by an up-down counter. This voltage is coupled through emitter follower, Q1, to the Darlington power transistor, Q2.

The collector of Q2 is connected through a 0.002-Ω current-sensing resistor to the load impedance, a 0.02-Ω resistive load with ∿0.2-μH inductance. Other regulator circuits can be connected in parallel to the load at this node.

A second input is supplied to amplifier A1 through potentiometer P1. This signal is the complement of the positive-going input to the D/A converter, and its purpose is to forward-bias Q1 and Q2 to overcome the base-emitter voltage drops of the transistors. With the counter cleared to zero, P1 is adjusted until an output just appears across the load.

Regulation is accomplished by a differencing amplifier, A2, a summing amplifier, A3, a dual differential comparator, and the up-down counter. Amplifier A2 extracts the difference signal across the 0.002-Ω current-sensing resistor. This signal is a measure of the Darlington collector current. It is necessary that A2 withstand the common mode voltage on its input terminals, a value equal to one-half the collector supply voltage when the Darlington is turned off.

The output from A2 is a negative-going pulse, having an amplitude proportional to the Darlington collector current. This pulse establishes a negative current through potentiometer P2, which is summed with a positive current proportional to the input-pulse amplitude. With I_{C1} at the desired value, P2 is

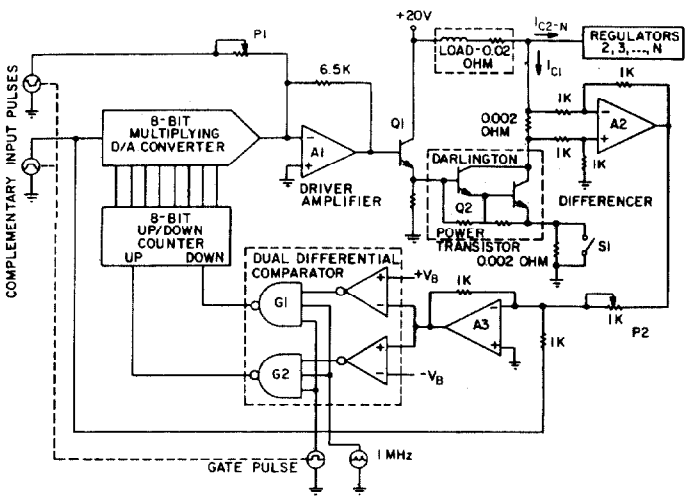

Fig. 4. Schematic diagram of the current regulator.

adjusted to produce zero volts at the A3 output. Should I_{C1} increase above the desired value, a positive pulse appears at the A3 output. Conversely, if I_{C1} is less than the desired value, a negative pulse appears at the A3 output.

The A3 signal controls the dual differential comparator as follows:

1. If the A3 output is zero, neither gate (G1 nor G2) is enabled, and the counter is held at its current state.
2. If the A3 output swings more positive than $+V_B$, gate G1 is enabled, allowing the 1-MHz pulses to be coupled to the counter's DOWN terminal. This reduces the count and lowers the drive to the Darlington, thereby reducing the collector current until the A3 output is less than $+V_B$.
3. If the A3 output swings more negative than $-V_B$, gate G2 is enabled, coupling the 1-MHz pulses to the counter's UP terminal. The count is increased, raising the drive to the Darlington and increasing the collector current until the A3 output is greater than $-V_B$.

A dead-band zone is supplied by $+V_B$ and $-V_B$ to minimize the comparators' noise triggering. For the experiment, these levels were set at +50 and -50 mV, respectively.

Gates G1 and G2 also are controlled by a gate pulse that is synchronized to the input pulse. This pulse allows the gates to be enabled only during the input pulse and minimizes transient effects during the pulse's leading and trailing edges.

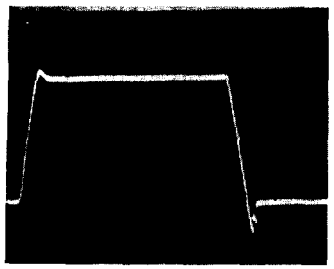

Fig. 5.
Two regulators supplying 200 A each.

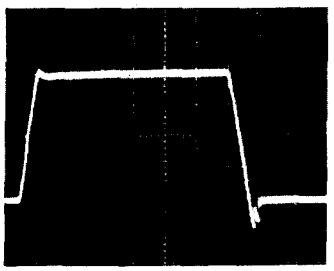

Fig. 6.
Two regulators supplying 200 A each with 0.002-Ω emitter resistor of Circuit 1 shorted.

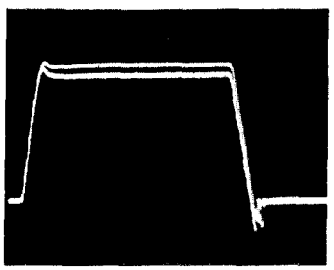

Fig. 7.
The effect of shorting the 0.002-Ω emitter register with the feedback loop opened.

The operation of two parallel-connected circuits is shown by the waveforms of Figs. 5, 6, and 7. The effect of transconductance difference in the transistors is simulated by a 0.002-Ω resistor and a switch, S1, connected to the Circuit 1 emitter.

Figure 5 shows a composite load current of 400 A, with each circuit supplying 200 A. In Fig. 6 the current remains essentially the same while the 0.002-Ω emitter resistor of Circuit 1 is shorted, indicating active regulation is taking place.

Figure 7 shows the effect of the emitter resistor when the feedback loop is opened and the regulation is disabled. When the emitter resistor is in the circuit, the current is 400 A. Shorting the resistor produces a current of ∿440 A. This step in current is regulated out when the feedback loop is closed (Fig. 6).

To improve the circuit response a microprocessor based regulator has been proposed as shown in Fig. 8. Here, the input signal and sensor signal will be converted to digital values and compared by the microprocessor. The appropriate digital outputs will be applied to the D/A converter to control the collector current of the Darlington power transistors.

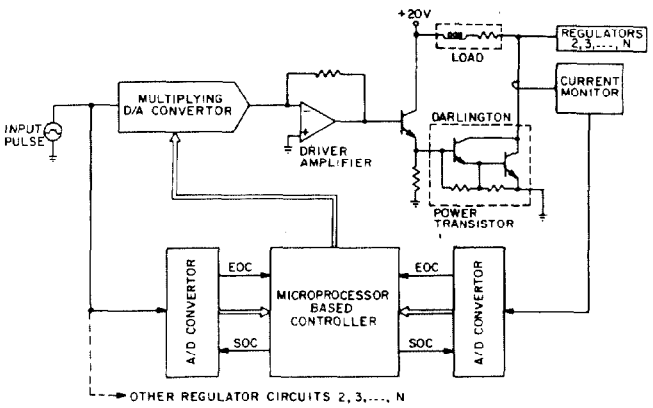

Fig. 8. Microprocessor-based current regulator.

Conclusion

A laboratory model of a current regulator based on individual V_{be} voltage control has demonstrated that this circuit can be a viable device for controlling current sharing among parallel-connected power transistors. Several aspects of the design that are still to be investigated are related to the transient response of the operational amplifiers, the nonlinear transfer function of the Darlington power transistor, and the design of energy-efficient power that would permit a larger duty cycle.

References

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2. J. W. McPherson, "Regulator Elements Using Transistors," Electronic Engineering, pp. 162-165 (March, 1964).