IMPROVED CONTROL SYSTEM OF THE THYRISTOR FLICKER SUPPRESSOR FOR THE KEK 12-GeV P.S.

S. Matsumoto, H. Baba, H. Sato, T. Sueno and K. Mikawa
National Laboratory for High Energy Physics
Oho-machi, Tsukuba-gun, Ibaraki-ken, 305, Japan

Summary

Thyristor control system of the 20 MVar flicker suppressor has been improved essentially. The previous feed forward (FF) loop with each single phase reactive current detector of the MR magnet power supply was exchanged to the present by both FF- and NFB-loops. The FF-loops consists of a three phase reactive power detector of the MPS and a forcing pattern generator on the fast but steady line voltage flicker, sag and surge. The NFB-loops control by the slow parts of the flicker and the unbalanced line voltages. These detectors of the reactive power, the voltage flicker and the unbalance have been developed. Sampled voltage flicker data with 12 bit ADC are processed by Z-80A micro computer system and the forcing pattern is generated by the system through 12 bit DAC into the loop. A typical voltage flicker including sag and surge has been reduced within ± 1.5 %, about 1/3 compared to the previous, at 66 kV primary line.

Introduction

Since 1953, the thyristor reactive power compensator (TQC)[1] has been powered up from 14 to 20 MVar, in order to reduce increasing reactive power attributed to load magnet saturations. On the routine 12 GeV operation, voltage flickers from the main ring magnet power supply (MPS) had been suppressed within ± 1.5 % at 66 kV power receiving point by the compensator except transient parts of pulsed voltage to MR magnets, referring to Fig. 1. The maximum voltage

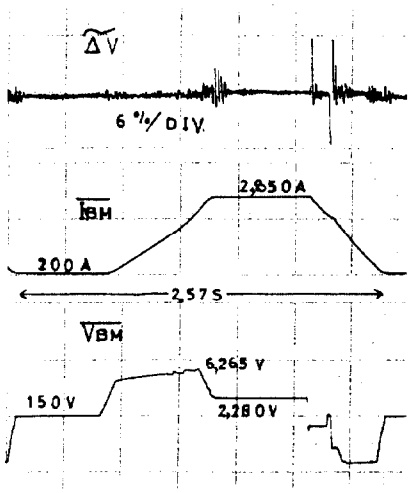

Fig. 1 Typical flicker and MR bending magnet current and voltage.

spikes (surge and sag) could be estimated at about ± 2 ∿ 4 % on the 66 kV line. These voltage spikes occur at the region just after the end of the flat top corresponding to the start of two-bridge-inverter-operation for the surge, and at the start of eight-bridge-inverter-operation for the sag, to release the stored energy in the bending magnets out to ac line. The rather strange operation pattern had come from a limit to reactive power compensation. The spikes have not given any sever disturbance to the beam spill of the 12 GeV machine, but may be harmful to other machines constructed or planned inside site of the laboratory. We aimed to improved transient characteristics and voltage regulation of the TQC.

Improvement

Fig. 2 shows a schematic diagram of the power and the improved control system. The TQC consist of 16 MVar bank with a rectifying transformer of Δ-Y winding and 4 MVar with Y-Δ winding. These 20 MVar lag power are compensated at the fundamental 50 Hz by capacitors in eight banks of harmonic resonant filter.

In the previous, the TQC had been controlled independently by reactive current of the MPS through open-loop on the every single phase to secondary windings of the 16 MVar and 4 MVar bank. In the loop, the transfer function should be requested a comparable accuracy to a desired level to suppress the voltage fluctuation as a control error. The function could be hardly determined in exact, because the whole system compose of the MPS, TQC, harmonic filters and the power line correlate in each other under large swing of active and reactive power.

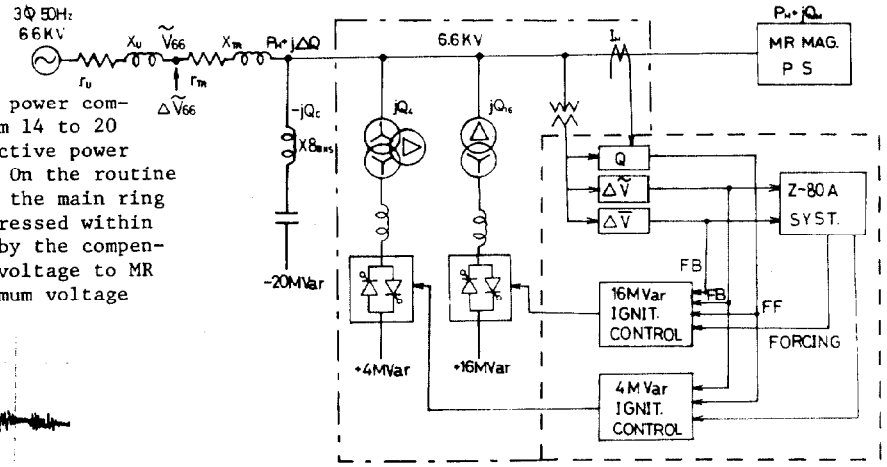

Fig. 2 Schematic diagram of TQC power and control system.

Predominant error source should be due to the tracking errors on the pulsed operation of the MPS by transient characteristics of the reactive current detector, of TQC thyristor, and coupled damping oscillation by a parallel resonance between large filter capacitors and source impedance of the line.

The improvements to the dead-time and the coupled oscillation would not be practical in cost performance, because the power system should be extended to the more multiphase operations.

We had intended to develop detectors on a voltage flicker ($\widetilde{\Delta V}$), on interphase voltage unbalances ($\overline{\Delta V}$), and on a reactive power (Q). The desired characteristics of the detectors were small transient to step input, fast and wide frequency response up to 300 Hz, and exact detection level less than 0.3 % inlcuding ripple components. These demands would be difficult to develop by simple analog circuits, as long as Q and $\widetilde{\Delta V}$ signals were processed on a single phase only.

However, the MPS was considered as a balanced load in the three phases to the TQC and to the power line, except transient regions. When the power source balanced among three phases, Q and $\widetilde{\Delta V}$ given by balanced load should be sum up to these of every single phase. This means that a loop controlled by the $\overline{\Delta V}$ detectors is necessary to make sure the interphase voltage balance.

On the other hand, in the transient regions, the load should have different patterns on every single phase, because of the transient characteristics of the

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power systems and of different capacity and operation mode among the 16 MVar, 4 MVar TQC and MPS. But large parts of the transient flickers are resolved to steady state components depended on the pulsed pattern of MPS. These fast but steady components are processed by μ-cpu system as a forcing corrector.

By these detectors, the control scheme does not only consist of FF-loops, but of NFB-loops. The FF-loops are regulated by the Q detector of the MPS and by the forcing patterns of $\widetilde{\Delta V}$ processed. And the NFB-loop by the $\widetilde{\Delta V}$ and $\overline{\Delta V}$ of the powered line.

Developed Detector

Analog Detector

A blief survey on the developed detector is given in the following.

The Q detector is the three phase sum output of single phase reactive power detector with analog multiplier of reactive current and voltage. The sensitivity is ± 10 Vdc to 20 MVar lag and lead.

The flicker detector $\widetilde{\Delta V}$ is an ac component of absolute value sum of 12 phase ac voltages. These voltages are composed of the weighted sums among the base three phase of the powered line. The sensitivity is 0.5 V for 1 % voltage change.

The interphase voltage unabalance detector $\overline{\Delta V}$ is an absolute sum of the base voltage and 60°- and 120°-delayed voltage through CR-phase shifter. Transient characteristics of the shifter have not any effect on the $\overline{\Delta V}$-loop within an open-loop gain 30 db, because of long first order lag with the time constant 2.0 sec. The sensitivity is 1.2 V to the 1 % unbalance.

μ-cpu System

The forcing corrector is a μ-cpu system with two Z80A to process for forcing pattern with sampled data of $\widetilde{\Delta V}$ signals at every 3.3 ms of zero cross timing of 3φ voltages. Fig. 3 gives schematic diagrams of the system. The one is main cpu, shown in Fig. 3a, supported by peripheral devices; CRT, Floppy Disk and printer. The cpu outputs the forcing pattern G_{x1} for 16 MVar and G_{x2} for 4 MVar TQC through 2-channels DAC. The other, given in Fig. 3b is sub cpu supported by control panel and ROM. The cpu controls ADC and multiplexor with four channels for $\widetilde{\Delta V}$, $\overline{\Delta V}$u-v, $\overline{\Delta V}$v-w and $\overline{\Delta V}$w-u as for control signals and with three channels as for monitor signals, magnet current I_M, 16 MVA TQC current I_{Q16} and 4 MVA I_{Q4}. Sampling rate for these signals except $\widetilde{\Delta V}$ is 10 ms interval. Fig. 4 shows timing schedule among these signals and other control signals. The three phase voltages on the top of the figure (a) indicate those of secondary winding of 16 MVar bank and the next three phase (b) mean those of 4 MVar. Tck (c) is the zero cross timing pulse of these 6φ ac voltage. T_{Rp} is a marker for positive polarity to synchronized phase with control period of the MPS.[2] P_1 is the beam injection start timing signal from the MPS. The sampled data of control and monitor signals are ordered to the P_1. After n pattern operations of MPS, sub cpu engages to calculate arithmetic mean on stored data of $\widetilde{\Delta V}$. Optmized weighted mean of several these data generate forcing pattern data for dynamical compensation of control delay in case of periodical inputs. The more exact algorithm had been discussed in case of the MPS operation.[3]

Performances and Discussions

In Fig. 5, typical results of voltage flickers by the monitors are given on a period of pulsed voltage to the bending magnet $\overline{V}_{BM}$, (a) controlled by the previous system, (b) by the present without forcing, and (c) by the present with forcing.

The flicker monitor signal is an ac part of a low pass filter output to three phase sum of absolute voltage for single phase in a monitoring line. Three monitors are used to measure the flickers in 66 kV, 6.6 kV utility, and the 6.6 kV line powered for MPS simultaneously. These monitors have been calibrated to the same input of the MPS line voltage for the outputs to have the same amplitude neglecting phase mis-match due to a small difference of low pass characteristics.

Slow components of the flicker are improved successfully on the MPS line comparing to the previous.

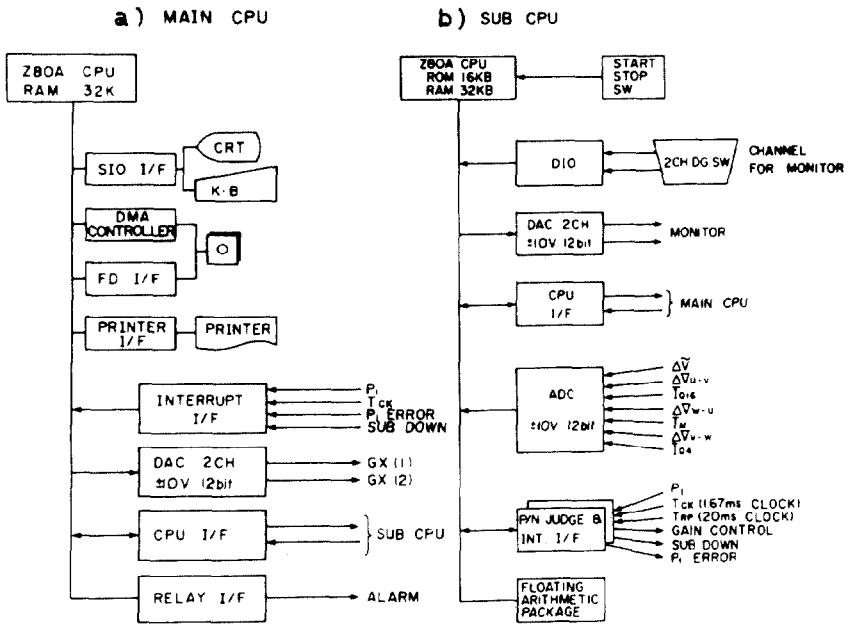


Fig. 3 Block diagram of μ-cpu system.

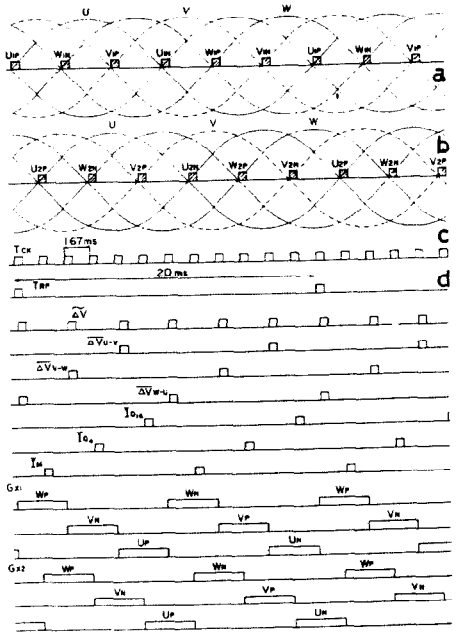
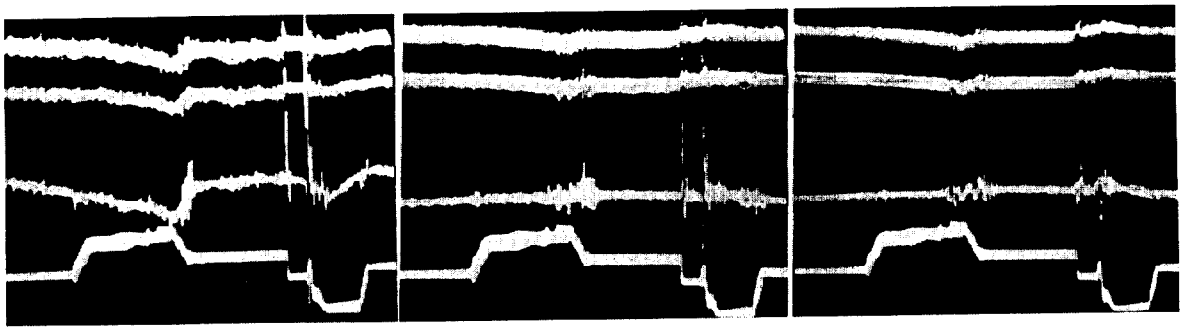


Fig. 4 Timing schedule of the control and monitor signals.



a) Previous b) Present without G_x c) Present with G_x

Fig. 5 Typical voltage flickers of monitor by different control schemes.

But, the components correlating the MPS have been still about 1 % on the 66 and 6.6 kV utility line, though the flickers decreased about 1/2 of the previous. Because the $\widetilde{\Delta V}$-loop works as a constant voltage regulator on the the MPS line, the ohmic drop by pulsed active power are compensated by lead reactive powers generated between the TQC and the harmonic filter banks. These reactive powers swing the 66 kV line through the source % reactance X_U. The voltage swing will be reduced, when quality factor q matching between the 66 kV and the MPS line.

$$\frac{r}{X} = \frac{r_U}{X_U} \quad \text{or} \quad q_{6.6} = q_{66}$$

where r and X are % resistance and reactance at the MPS line and r_U is % resistance at the 66 kV. The more detail discussions will be described some place.

On the fast components, the sag would be estimated at about a half compared to the previous, but surges are nearly equal to the previous. These spikes reduce on the 66 kV to 1/3 proportional to X_U/X as given in Fig. 5(a) and (b). Fig. 6(a) and (b) indicate more clearly for the ratio to be the same within some ambiguities by ripple of 100 Hz.

Fig. 7 gives developed detector and monitor signals of $\widetilde{\Delta V}$ with and without forcing loop. The developed signals have very noisy higher order harmonic components and fast response. On the other hands, the monitor could not resolve higher component than 100 Hz. In Fig. 7(a) and (b), the flicker are given without forcing loop. And in Fig. 7(c) and (d) with forcing loop. These results indicate for the forcing loop to reduce the flicker to about a half at least.

By the forcing, the higher components than 100 Hz generate or have still a considerable level but within

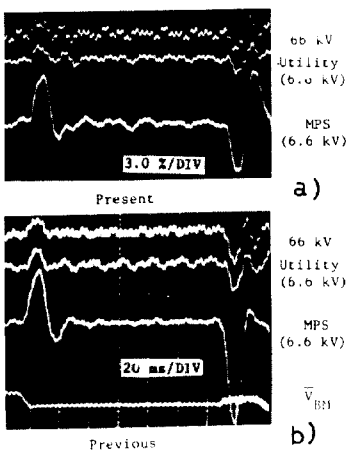


Fig. 6 Maximum surge and sag.

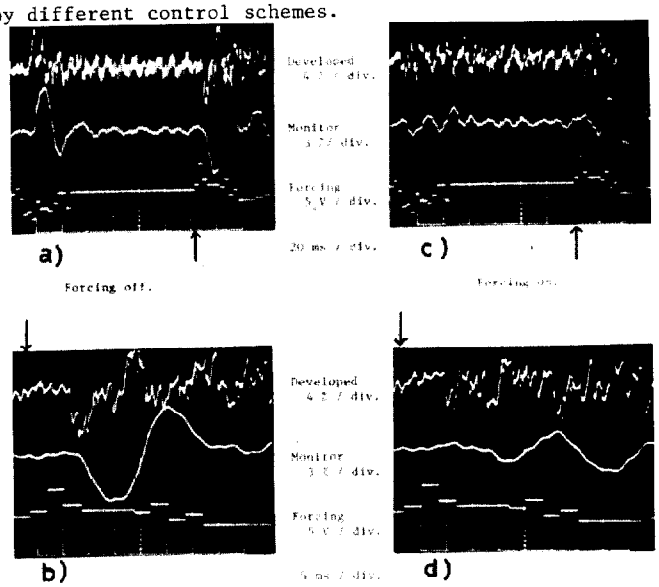


Fig. 7 $\widetilde{\Delta V}$ and G_{x1} signal.

± 4 %. These control error would be account for lack of compensation capacity of TQC and for failure to find out the optimum weights for the forcing pattern. On the 66 kV line, the contribution of such higher components might be never important to practical limits to the flicker, but rather slow component would be injurious, if residual had a larger level. As a result, the residual flicker derived from the MPS would be estimated at within ± 1.5 % including slow and fast components on the 66 kV line.

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