IEEE Transactions on Nuclear Science, Vol. NS-30, No. 4, August 1983

APPLICATION OF A DIGITAL TRIGGER GENERATOR TO NSLS BOOSTER AND STORAGE RING DIPOLE POWER SUPPLIES*

B. B. Culwick and R. E. Olsen
National Synchrotron Light Source
Brookhaven National Laboratory, Upton, N.Y. 11973

Abstract

The digital trigger generator described in reference (1) has been used to control a number of power supplies at the NSLS. Two extensions to the basic controller have been used to preserve its inherent high performance in particular applications. In the case of fast slew rate applications, the bandwidth limits of the supply generate errors in tracking the current reference. The repetitive nature of the NSLS Booster cycle has made possible an adaptive feed-forward scheme which corrects the errors of a given cycle based on data derived from previous cycles. For slowly varying current regulated supplies, the residual subharmonic ripple due to unbalanced phase voltages, transformer unbalance, etc. is corrected by means of a microprocessor based harmonic analyser which feeds data to the phase correction input of the controller.

Introduction

The paper in reference (1) describes the design features and functioning of a digital trigger generator for large SCR power supplies. The trigger generator has been applied in the control of a number of power supplies within the National Synchrotron Light Source project. Two classes of applications can be identified:

1) Power supplies in which a moderately accurate output current is required to vary at a rate not negligible with respect to the bandwidth of the controller, typified by the Booster dipole power supply.

2) Power supplies in which a precisely controlled output current varying slowly with respect to the bandwidth limit of the controller is required, typified by the storage ring dipole supplies.

Application to the Booster Dipole Power Supply

This application supplies a current of 150 A to 1600 A with a precision of ~ 0.1% to a load of 0.05Ω in series with 0.1 H. The current is required to slew over the full range in 0.2 S. The static precision requirement is easily met by the trigger generator but, since the natural time constant of the load is 2S and that of the rectifier, a 6 phase, 12 pulse system, is ~ 3 mS serious current lags occur for slew time constants less than 1 S. This limitation is overcome by making use of the fact that the Booster synchrotron operates in a repetitive cycle with a period of usually ~ 1 S. The controller is implemented with a voltage feedback loop of gain 50 rolled off at 2.3 Hz. A current feedback loop of gain 1800 is used, rolled off at 0.08 Hz by the time constant of the magnet load. The output lag due to these time constants is corrected by a device called the Adaptive Equalizer. This operates as follows: during each cycle the output error, which may be sampled anywhere in the forward loop, is digitized at a 720 Hz sampling rate. The resultant value at each sample is scaled and added to the contents of a 4 K word memory at a location corresponding to the time within the cycle. During each cycle, the contents of the memory at the appropriate locations are converted to analog values and summed into the error amplifier. The result is that, over some cycles, the errors occurring in previous cycles are integrated out at a rate depending on the scaling factor and the number of cycles. The effect is similar to lag compensation applied in a continuous fashion to a non-repetitive supply, but uses the experience of previous cycles to correct the current cycle. Practical values of the constants permit reduction of the slew induced errors from ~ 1% to < .05%. The performance with and without the adaptive equalizer for the Booster dipole supply is illustrated in Figs. 1 and 2.

Storage Ring Dipole Power Supply Application

The design objective of the 700 MeV storage ring dipole power supply is to control a current of 300 A to 2000 A with a precision of 0.01% into 0.05Ω in series with 0.1 H. The slew rates required are modest, typically 20% of range in 300 S. The adaptive equalizer described above can be modififed for non-repetitive operation by using a single memory location or conventional analog lag compensation can be used to reduce slewing errors to very low values. Under these circumstances, the principal errors in dipole magnetic field are due to subharmonic ripple components in the output voltage of the supply. The 720 Hz ripple voltage in the 6 phase, 12 pulse rectifier at normal outputs is of the order of 100% producing a ripple current in the load of ~ 0.2 A. Moreover, this is further reduced by an LC filter to ~ 0.01 A. Subharmonic frequency components of ripple voltage produce relatively larger current amplitudes for a given ripple voltage, are more difficult to filter and such filters degrade the servo performance. Subharmonics of the 12 pulse frequency are present, even if the timing control is perfect, due to unbalance in the incoming line phases, in the transformer and in the individual phase components of the rectifier. The trigger generator makes provision for corrections to the individual firing angles to correct these effects. Corrections can be applied statically for permanent sources of errors, eg. impedance unbalance. Dynamic errors due to line disturbances, temperature variation and aging of components must be compensated dynamically. In this design the output voltage is processed by a harmonic analyser and the necessary corrections fed to the phase correction inputs. The output voltage amplitude of the supply is sampled by a synchronous analog to digital converter triggered at a multiple of the 720 Hz power supply triggering frequency. A multiplier of 16 was selected giving a sampling frequency of 11520 Hz. The digital outputs are summed into a binary adder during each phase of the supply operation. At the end of each phase period, the sum is transferred to a microprocessor which computes the amplitude of this phase with respect to the average of all phases. A timing correction for the phase is computed and added to the previously computed value for this phase. The new value of the timing correction is transferred to the trigger generator via the phase correction input. A block diagram is shown in Fig. 3. Since a time delay of 1/60 S is inherent in the correction procedure, the gain bandwidth product is limited to < 60, but slowly varying phase to phase errors can be compensated to any reasonable accuracy.

* Research supported by the U.S. Department of Energy.

0018-9499/83/0800-2865$01.00©1983 IEEE

The correction system has been tested using a simulator module to manually load data to the correction memory. The microprocessor portion of the correction logic is designed and under construction.

Acknowledgement

We gratefully acknowledge the expert advice and assistance of A. V. Soukos in the design of the analog servo and testing of the high power components.

Reference

1. A high performance digital trigger system for phase controlled rectifiers, R. E. Olsen Paper Y7 in this conference

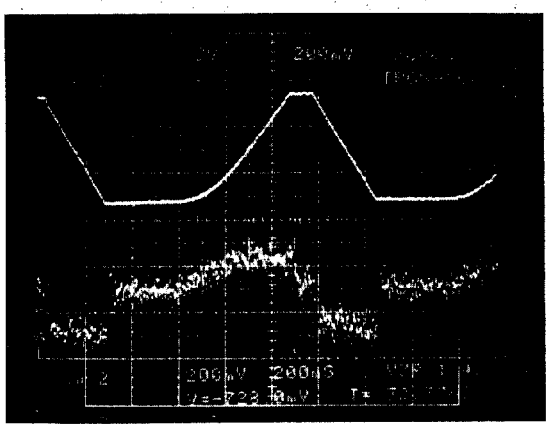

Fig. 1. Ramp and Error signals for the Booster Dipole without the Adaptive Equalizer.

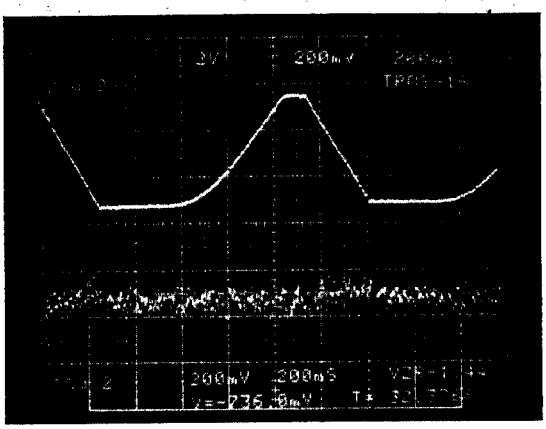

Fig. 2. Ramp and Error Signals for the Booster Dipole with the Adaptive Equalizer Connected.

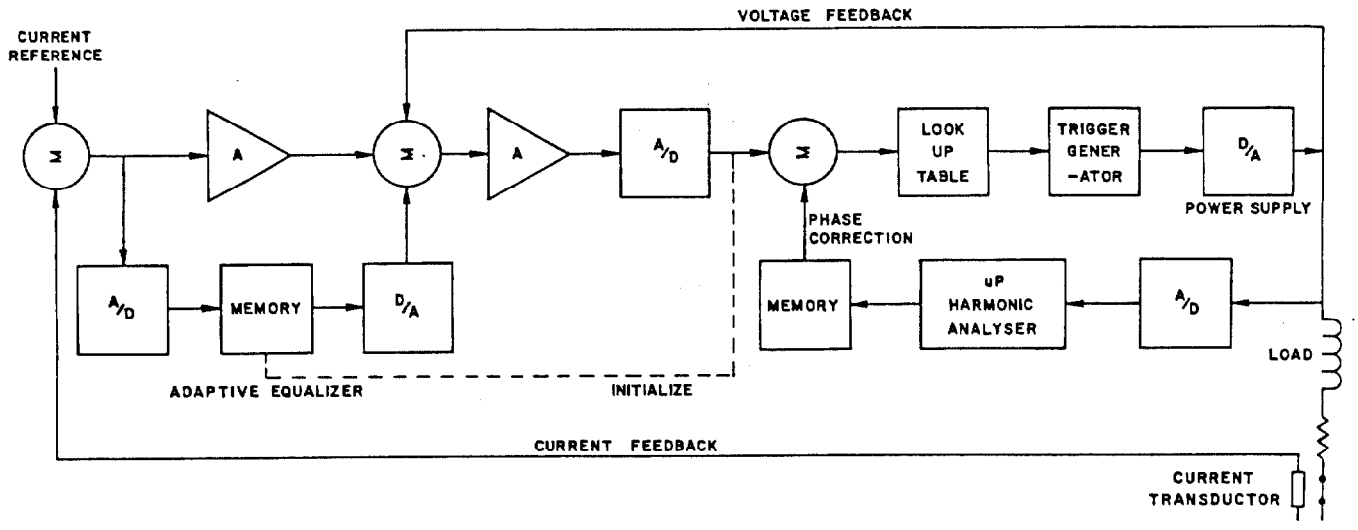

Fig. 3. Functional Block Diagram of the VUV Dipole Power Supply.