APPLICATIONS OF FASTBUS TO BEAM DIAGNOSTICS AND EXPERIMENT DATA SYSTEMS

Donald R. Machen
Scientific Systems International*
Los Alamos, New Mexico 87544
USA

Summary

A five-year effort by the North American NIM Committee, in collaboration with the ESONE Committee of European Laboratories, has resulted in a specification for the FASTBUS modular, high-speed data-acquisition system.[1] The system is designed around an emitter-coupled logic (ECL) 32-bit data bus for asynchronous data transmission at 100 ns per transaction. Initial applications of FASTBUS will be in experiment data systems at accelerator facilities worldwide--beam diagnostic data systems on the accelerator side and particle-beam experiment data systems in the experimental area. As the specification (and the resulting hardware and software) matures, real-time machine-control applications will become possible. The FASTBUS specification has been proposed to the Institute of Electrical and Electronic Engineers (IEEE) for standardization in the United States (IEEE-P960), and the specification will be submitted to the international standards bodies for standardization on a worldwide scale in the near future. The details of the new standard are discussed by Costrell and Dawson[2] at this conference.

This paper will discuss the near-term use of FASTBUS in accelerator beam-diagnostics instrumentation systems, where an extra increment in system throughput and front-end processing speed can produce a greater understanding of the physical phenomena under study. The arguments and conclusions may be equally well applied to other similar data-handling problems requiring high bandwidth in the data system.

Introduction

The technological advances in the machines of physics and in the detectors commonly used for studying the fundamental processes involved (not to mention the advances in the electronic devices used to gather and process the related information) have resulted in a dependency upon digital data-handling and processing techniques in the physical sciences. The need to understand the machine and its product is essential and only possible by direct parametric measurements of the particle beam, or by indirect measurements of the interaction products. Further, the process of understanding the phenomena involved with either particle beam production or usage requires an ever-increasing data rate and data volume and a significant amount of data processing prior to final data reduction. Often the process must occur in real time or as near to real time as possible in order to attempt an understanding of the problem or experiment. The allowed beam time and available funds are other constraints that help to create the need for better, faster, and more capable digital data systems.

The illustration in Fig. 1 indicates the general configuration of a digital data-acquisition system with a bus structure for data multiplexing and transmission of the data through an interface to a computing system. The computing system, in this case, is used for final data reduction and possibly intermediate bus control. Further, a number of data-bus standards have been noted, which indicates that there may be more than one solution to the question of which data system to use!

As semiconductor electronics and the microprocessor have evolved, so has the data-transmission bus structure; the bus width has progressed from 8 bits through 16 bits to 24 bits, and now 32 bits seems to be an acceptable norm. The synchronous bus was common in the early days, but the asynchronous, multiplexed bus is now the more accepted technique in implementation. Of course, there have been many examples of special implementations for specific problems in which a more optimal design seems to address a particular aspect of a data-collection or reduction problem.

A particular advantage for the experimenter when a standard bus structure is selected is the possibility of useful I/O devices or interfaces existing either commercially or at other similar facilities elsewhere. The engineering time required to complete a specific data-system design can often be reduced considerably.

A significant requirement of many beam diagnostic or experimental physics instrumentation problems is the increasing need for local, high-speed data preprocessing. Several of the digital data-bus standards noted in Fig. 1 were a product of a specific microprocessor structure and therefore reflect many of the features of those microprocessors.

These buses will generally accept single or multiple processors on the data bus, thereby allowing the experimenter to split the computational load between the experiment computing system and the real-time input/output "front-end" processor(s). A discussion of front-end processing in the CAMAC standard is contained in Ref. 3.

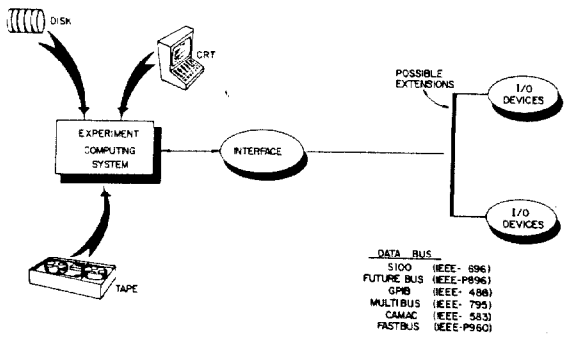

Fig. 1 A Typical Data Acquisition System

* 3491 B Trinity Drive; a division of KineticSystems Corporation, Lockport, Illinois 60441 USA

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The FASTBUS Data System

The new FASTBUS modular data-system standard has provided the necessary framework in which experimenters may place device electronics in ECL and expect a 320-mbps maximum transfer bandwidth over the bus structure (called a Segment in the FASTBUS specification). The 320-mbps bandwidth of the FASTBUS segment is in contrast to the previous highest bandwidth available in standard bus structures of 24 mbps (CAMAC). Other well-known bus standards exhibit maximum bandwidths less than this figure. The illustration in Fig. 2 indicates how an experimenter could configure a FASTBUS data system for a beam diagnostic experiment; the experiment would probably be one for which conventional data acquisition structures are inadequate owing to an insufficient maximum bus speed, a bus width that is too small to maintain precision or to address a large-enough bulk store, or a limitation of the structure in available physical space for I/O devices, or some combination of these particular inadequacies. The configuration illustrated in Fig. 2 could provide a solution to the problem mentioned above, in addition to being a more easily understood FASTBUS configuration for the first-time user.

The many technical details and salient features of FASTBUS are well covered in Ref. 1 and discussed in Ref. 2 and will not be discussed here. Instead, a simple topology being developed for the first-time user or for the medium-size FASTBUS system will be described.

A FASTBUS System for Beam Diagnostics Data Systems

Interfaces from computing systems to FASTBUS have begun with the very simple (and slow) devices and have proceeded to the quite complex, high-speed, list-processing, block-transfer controllers. The first-time user may require an interface that could be operated in a standalone configuration from a simple CRT terminal. The initial data processing is accomplished at FASTBUS speeds by a FASTBUS Front-End Processor (FFEP), while the interface is needed to extract a block of preprocessed data and to send the data to the computing system memory, if a central computing facilty is used at all. When the interface is being operated in a standalone mode, it is capable of executing a prestored list of FASTBUS instructions, which includes reading, writing, and controlling instructions. The great benefit for the accelerator experimenter, however, is the capability of the bus structure to operate at a rate that exceeds commonly used data-systems electronics by an order of magnitude. Block-cycle transfer rates can approach 50 ns per operation, while normal random-access cycle rates proceed at 100 ns per transaction. The FASTBUS structure accommodates high-speed ECL electronics (in addition, TTL and analog electronics may be mixed with ECL); the immediate consequence is that ECL front-end processing hardware is supported and planned for experimental use. An ECL data-processing device (microprogrammed facility) is able to acquire and manipulate data from ECL I/O devices along an ECL data bus; the result of such a marriage of high-speed devices is that maximum data-handling bandwidth is available for the first time in a modular configuration. Data handling by ECL devices has been used for special-purpose physics instrumentation for some years and by the Cray Computer Company in the Cray I computer for scientific calculations. As a result of FASTBUS, the higher-speed devices are now available to the experimenter for data-acquisition purposes.

The last point of interest in the discussion of FASTBUS systems for the first-time user is the expansion of the single crate to multiple crates either when the experiment is physically spread out or when the number of devices exceeds the space available for inserting them in the bus. The illustration in Fig. 2 indicates a coupling device between each physical bus. The more complex FASTBUS system will use a defined Segment Interconnect (SI) to perform a general connection and allow master devices (processors) to be placed in any FASTBUS crate (bus). For the simpler, less involved FASTBUS system, a Segment Extension (SE) is being considered. The SE allows multiple crates to be connected together in an "extended-crate" FASTBUS configuration, but master devices are only accepted in the first crate, along with the arbitration timing logic (ancillary logic, see Ref. 1). The number of FASTBUS I/O devices permitted is then increased by 26 for each crate added (a practical maximum is in the order of four crates), as the cycle time is also extended by 10-20 ns with each

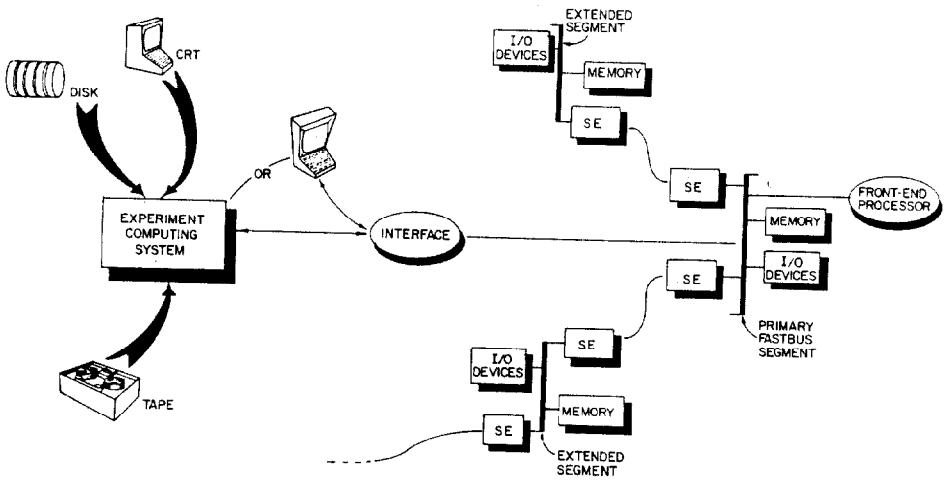

Fig. 2. Extended FASTBUS Data Acquisition System

extension. The SE would not require the elaborate initialization that the SI requires; however, only a subset of the FASTBUS functions would be available on the extended Segments.

Once the SEs have extended the physical space available in a single-crate configuration, the FASTBUS system may begin to support a large quantity of bulk-storage modules (for instance, 1/2 mbyte memories) for both raw and preprocessed data. The 32-bit address space of the FASTBUS specification allows more than 800 mbyts of storage if needed. Depending upon the experiment application, this memory may be used as FFEP memory (data, not program), allowing entire graphic distributions to be assembled for many parametric conditions.

Conclusions

The application of the new, high-speed modular data acquisition system, FASTBUS, to beam diagnostics problems has been described. A less involved configuration directed to the first-time user, or to the experimenter not requiring the full capability of the FASTBUS system, is also being considered for commercialization. The FASTBUS system configuration permits the use of fast preprocessors, large memories, acquisition devices (ADCs, input registers) and standalone or connected interfaces in an extended-crate arrangement. The extended-crate arrangement is simpler and less involved than an interconnected arrangement that uses the full-capability Segment Interconnects.

References

1. FASTBUS: Modular High Speed Data-Acquisition System for High Energy Physics and Other Applications, U.S. NIM Committee, November 1982.

2. Louis Costrell and W. K. Dawson, "FASTBUS for Data Acquisiton and Control," to be published in the Proceedings of this conference.

3. D. R. Machen, "High Speed Front-End Processing in CAMAC Interface Systems," Interfaces in Computing, Elsevier Sequoia SA Lausanne, Switzerland, Vol. 1, No. 1, May 1982, pp. 75-83.