

## A NEW CONTROL SYSTEM FOR THE SLAC ACCELERATOR KLYSTRONS FOR SLC\*

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### Summary

A general overview of a new control system for SLAC klystrons is presented along with a detailed description of the remote controller for measurement and control of accelerator components.

### Introduction

Various properties of the RF sources for the SLAC linear accelerator will be measured on every pulse by a system currently being developed. The system is broken into four major parts: A new computer control system, a new timing system, a new remote controller, and new remote RF and Analog heads (see Fig. 1).

#### Control System

The SLAC accelerator is being instrumented with a new control system which is based on a VAX main computer with a large number (~ 100) of remote computing nodes. Each node features an Intel 8086/87 micro computer connected to the host by a broadband CATV communications system (SLC-NET). The remote processors (cluster micros) control all devices in a geographically designated area. The cluster micro communicates with all peripherals through a new serial CAMAC channel supporting up to 16 crates. The cluster micro is responsible for monitoring all magnets, beam position monitors, klystrons, digital control/status, linac temperatures, and analog voltages. The high speed control of klystrons is done by a Parallel Input Output Module (PIOP) resident in CAMAC.

#### Timing System

The timing of all accelerator systems is derived from a new timing system based on a Programmable Delay Unit (PDU). The PDU is a 16 channel digital delay unit that operates in the CAMAC environment. The accelerator's 476 MHz main drive line is the frequency source for all timing delays. A fiducial superimposed on the main drive serves as a system trigger. The PDU detects the fiducial and counts cycles of a 119 MHz sub-harmonic of the main drive to generate timely triggers on a special CAMAC upper-backplane buss.

#### Remote Controller

The PIOP is an 8088 based controller designed for the high speed control and monitoring of the pulsed accelerator klystrons at SLAC. The processor is interrupt driven, and monitors all signals of interest every 2.7 milliseconds.

The PIOP is connected to the klystron through a SLC standard 18 pair digital cable. The cable contains necessary timing information to trigger and monitor the klystron and a data buss to allow the required controls. (The PIOP is discussed in detail in this paper.)

#### Remote Head

The remote heads for use with the PIOP contain all the analog and RF circuitry. The timing for any sampling is derived from the PIOP via the differential cable. The firmware in the PIOP will, upon receiving an interrupt, read the head and assert any new values that will be required for the next klystron pulse. Two heads are currently being developed for the SLAC klystrons: The Phase and Amplitude Detector (PAD) to measure the klystron's RF output, and the Modulator Klystron Controller (MK-2) designed to provide all the necessary protection, monitoring, and control for the current SLAC high power pulsed klystrons. The two heads are designed to operate in parallel off the same PIOP controller, allowing a single controller to monitor ALL aspects of a klystron's performance.

#### Control System Requirements

The Stanford Linear Collider (SLC) project underway at SLAC is placing stringent requirements on the quality of control and monitoring of all accelerator sub-systems. The requirements for klystrons fall into two general classes: Monitoring of defective RF pulses, and Instrumentation and Control.

#### RF Performance

The monitoring of sub-standard RF pulses will be critical to the high bandwidth servo systems steering the beam for SLC. The servo controllers must be informed of every sub-standard pulse from every klystron to allow the servo algorithms to discard the most affected data point.

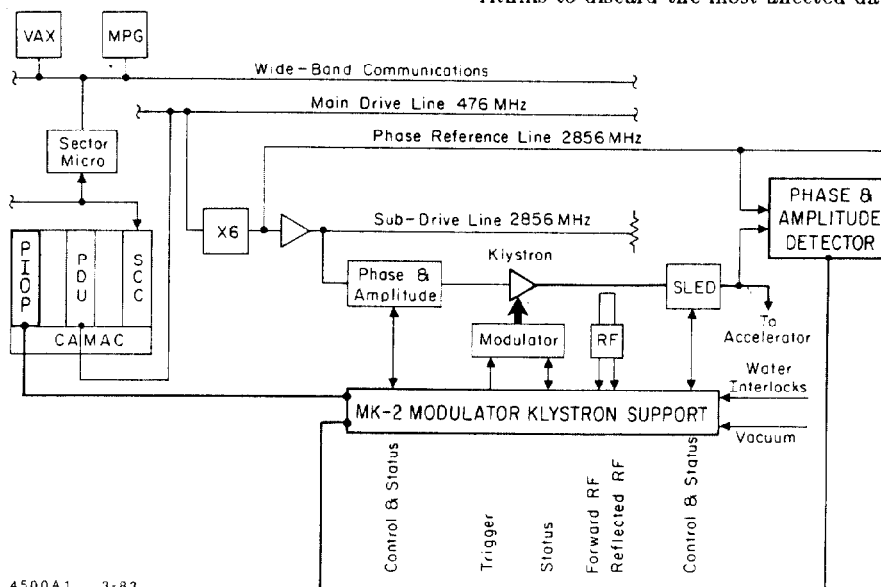


Fig. 1. Instrumentation for a typical klystron.

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## Klystron Instrumentation

The Instrumentation and Control upgrade of the existing klystrons will provide the accelerator operators with complete information of the status of each klystron station.

This upgrade will include new solid state adjustable input attenuators for the RF drive to each station. The new attenuators maintain a virtually constant RF phase output of the klystron over the desired range of attenuation. This upgrade will allow maintenance personnel to saturate the klystrons without seriously interfering with machine operations.

### General Overview of the PIOP

The PIOP is schematically presented in Fig. 2.

#### PIOP Services

The PIOP will have in a buffer available for asynchronous reads containing critical status information. In addition, the PIOP will provide the control system with a number of diagnostic programs. The information and services are:

1. Instant access to klystron phase, amplitude, and status.
2. Ability to service klystron at 360 Hertz, allowing all measurements to be made for every pulse.
3. Control responsibility of 300 klystrons removed from main control system.
4. "Fast Time Plot" sampling scope type waveform analysis of all time dependent signals. Data is collected by sampling the waveform at different times on each of 64 sequential pulses. Sample delay and interval are specified by the control system. Timing is generated by counting half-cycles of 14.875 MHz (33.6 nanoseconds) (see Fig. 3).
5. Errors are reported using the CAMAC "LAM" and the 16-bit CAMAC Message buffer.

## PIOP Hardware Description

The PIOP is a single width CAMAC module which is controlled by an internal microprocessor. The microprocessor controls three major ports on the PIOP: Timing, CAMAC, and a Remote Head.

Timing information is received through the special upper backplane buss on all SLC CAMAC crates. The Processor selects a channel from the buss, and delivers the selected triggers to the remote head.

CAMAC information is transferred by either of the single word buffers, or by a special block protocol. The CAMAC data is stored in a multi-ported memory, and is freely available to the micro processor. Block transfers are done using a DMA support device, with all necessary pre-fetching and data storage done by system hardware. Block sizes and access are controlled by the processor (see Fig. 4).

The "REMOTE HEAD" is connected to the PIOP by a special link connection on the module's front panel. The link features a 256 byte memory mapped port directly available to the processor. A trigger and a clock, both synchronous with the accelerator beam, are also available on the link. An external interrupt has been provided to allow for expansion for future needs. Communication with the remote head halts the micro processor until an acknowledge from the peripheral device is received, allowing for extended cable runs and slow digital sources. A 50 micro-second timeout has been provided to allow the processor to gracefully recover and diagnose a defective head.

#### Processor Summary

The major features of the micro processor are summarized below:

- Intel 8088 processor running at 5 MHz. The 8088 is an 8-bit buss version of the popular 8086 16-bit processor.

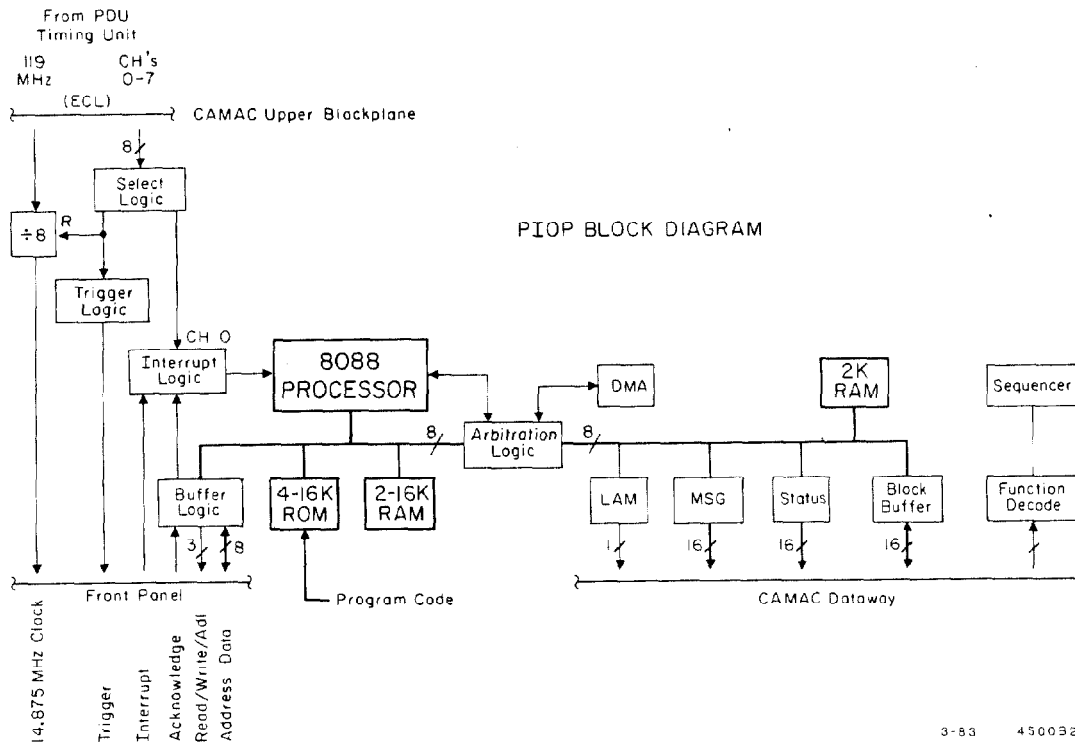


Fig. 2. PIOP block diagram.

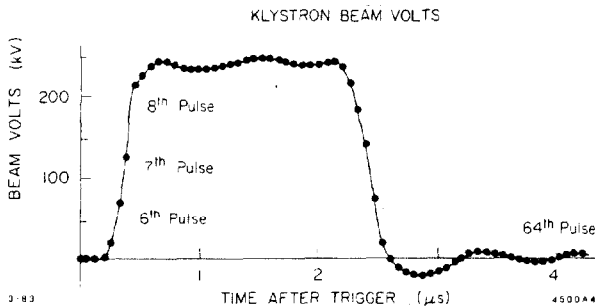


Fig. 3. Example of a fast time plot.

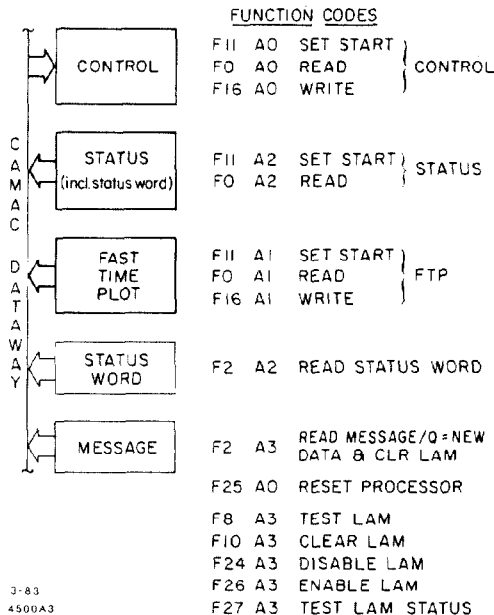


Fig. 4. CAMAC function codes.

- Programs stored in on board EPROM memory. Programs up to 16 K Bytes can be used.
- Programs are written in PL/M-86 and compiled on a VAX/VMS.
- Processor ROM is 2 to 18 K Bytes, depending on memory chips selected.
- CAMAC buffers, System Flags, and Remote Head are all memory mapped.

### Remote Head Summary

- All signals are differential TTL.
- An 8-bit address/data buss uses the industry standard address latch protocol.
- The processor is halted on remote head accesses until an ACKnowledge is received.
- ACKnowledge may be delayed up to 50 microseconds to accommodate slow digital sources such as analog to digital converters
- Read and Write timing is not critical.

### CAMAC Summary

- CAMAC buffers are all 16 bits wide.
- Three programmed length blocks are accessible by CAMAC. The usual configuration follows:
  - Control Block is 16 words long and used to write command blocks to the PIOP.
  - Status Block is 32 words, and contains status information of the klystron. The structure of this block is fixed, allowing asynchronous reads.
  - FTP Block is 67 words long. This block is used to contain information specifically requested by a command previously written in the control block.
- Two single word buffers exist:
  - Status Word contains summary information on the klystron.
  - Message Word is a message buffer used to deliver messages of klystron faults. If the module's "LAM" is enabled, "L" is asserted when this buffer contains new information.
- Several Commands exist:
  - Reset provides a hard reset of the processor.
  - LAM controls are fully supported.

### Acknowledgement

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### References

1. "Applications of Local Area Networks to Accelerator Control Systems at the Stanford Linear Accelerator," J. D. Fox, E. Linstadt, and R. Mellon, these proceedings.
2. "Phase and Amplitude Detection System for the Stanford Linear Accelerator," J. D. Fox, and H. D. Schwartz, these proceedings.
3. "Stanford Collider Wide-Band Control and Monitoring Network," W. Struven, these proceedings.