A MULTI-CHANNEL FIBRE-OPTIC LINK FOR ANALOG TELEMETRY

M.R. Shubaly and J.G. Plato

Atomic Energy of Canada Limited, Research Company
Chalk River Nuclear Laboratories
Chalk River, Ontario, Canada K0J 1J0

Summary

Control of an ion beam injector requires a reliable telemetry link for analog signals between the high voltage dome and ground. This paper describes a self-scanning, self-checking system capable of transmitting up to sixteen channels of analog data (in each direction) with eight bit resolution over a dual light link. The technique used is serial transmission of eight bit words using standard UART's (Universal Asynchronous Receiver Transmitter) which provide much of the error detection and timing. Two versions, one stand-alone for manual control, the other an input/output interface board that plugs into a control microcomputer, have been designed. For sixteen channels, the data is updated every 3.2 milliseconds. The simple design and low parts count provide a low cost analog telemetry system.

Introduction

The control interface between ground and the high voltage dome of ion injectors has been addressed in several ways. One technique is to use insulated rods to transmit control to power supplies in the high voltage dome and large, easily read meters to transfer the information back to the operator. Such a system is clearly unsuitable for computer control, where a better solution is to use fibre-optic cables and transmitter-receiver units. For the injectors currently being developed at Chalk River, we require:

1. Up to sixteen analog channels and eight on-off channels (for switching and status indication) in each direction.

2. Better than 1% linearity and resolution for analog channels.

3. Channel update times of less than 10 ms (based on a typical SCR power supply response time of 50 ms) to permit the link to be used in the control loops of the plasma generator power supplies.

4. Fast detection of loop failure or transmission errors because of possible effects of spark induced transients and the potential for serious damage if the link fails.

We have chosen to use digital transmission because of linearity limitations with large bandwidth analog telemetry, and multiplexing to minimize hardware costs. The light link described in this paper satisfies these requirements and is, in addition, inexpensive and easily configured for various applications. The cycle time is over 250 times faster than that of a multiplexed fibre-optic link described recently[1]. Component cost for a sixteen channel unit, less enclosures and power supplies, is $600.

Description

Two different ground station (master) units have been developed, each using the same high voltage dome (slave) unit. The master described in detail below is a stand-alone unit. The second master is designed as an input/output board which plugs into the back plane of the injector control microcomputer. Both versions have a common basic circuit. A block diagram of the stand-alone master and slave is shown in Fig. 1. Up to sixteen channels are available, with the first channel selectable as analog or digital (giving eight control bits).

Communication takes place through UARTs (Universal Asynchronous Receiver Transmitters) at either end of the light link that provide much of the system timing and error detection. Each UART contains a transmitter that is loaded in parallel from an eight bit data bus with a word which is then sent out, in serial form, with added start, stop and parity bits. Use of such a device allows a considerable simplification of the circuitry. Timing and clocking of channel counters is controlled by the Transmitted Data Strobe (TDS) and Received Data Available (RDA) signals from the UART. Figure 2 shows some of the timing signals. A UART cycle is the time required to send or receive one complete word; a frame is composed of "n+3" UART cycles, where "n" is the number of channels. The master is free running - sending to the slave the selected number of channels of data, followed by three UART cycles with the up-link (from master to slave) held in the mark (illuminated) state. The slave starts tranmission to the master when it receives the first data word in the frame. The slave sends its status

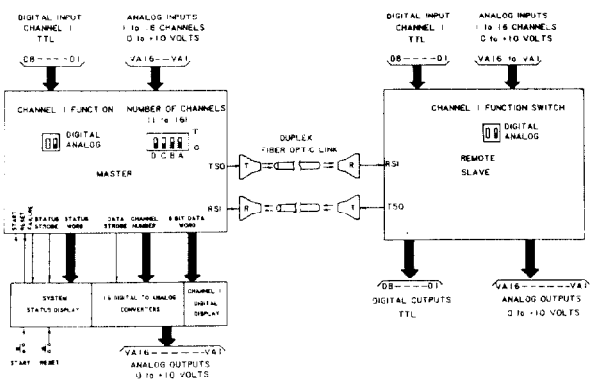

Figure 1. Block diagram of light-link, stand-alone version.

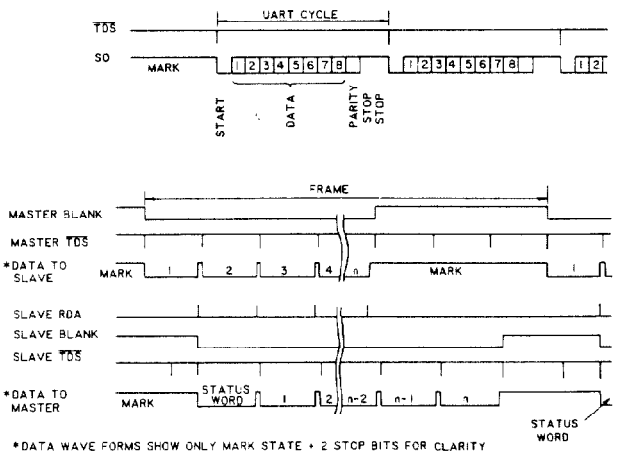

Figure 2. Timing diagram.

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word, followed by the same number of channels of data that it received. The three cycles in the mark state of the up-link are needed to allow the slave to complete its transmission before the master sends the next data frame.

Figure 3 is a block diagram of the slave. On power up, the slave sets the outputs of the digital-to-analog converters (DACs) to zero. It then sends a status word, followed by the value measured by the first channel. If the slave does not receive data from the master, it will set a flag called BLANK, zero the outputs of the DACs and start another cycle. In normal operation, the first data received from the master will clear the BLANK flag, reset the receiver counter, reset the event counter and, if no transmission errors (parity, framing or over-run) have occurred, load the received value into the DAC for the first channel. If an error does occur the value stored in the DAC is not changed. The UART is reset (to provide synchronization), and a status word (showing parity, over-run and framing errors from the previous cycle) is loaded and sent. Subsequently received words advance the receiver counter and, if error free, are loaded into the DACs. At the end of the transmission of the first word (the status word) the first channel of analog data is loaded into the UART and sent. After each word is sent, another word is loaded and sent until the slave has sent one more word than it received. When it tries to set the next word, the BLANK flag is set and the optical transmitter goes to the mark state. If a data word is not received during the next UART transmit cycle, a communication failure is assumed and the slave goes to the reset state. If a new data word is received (as is normally the case) the frame starts over again.

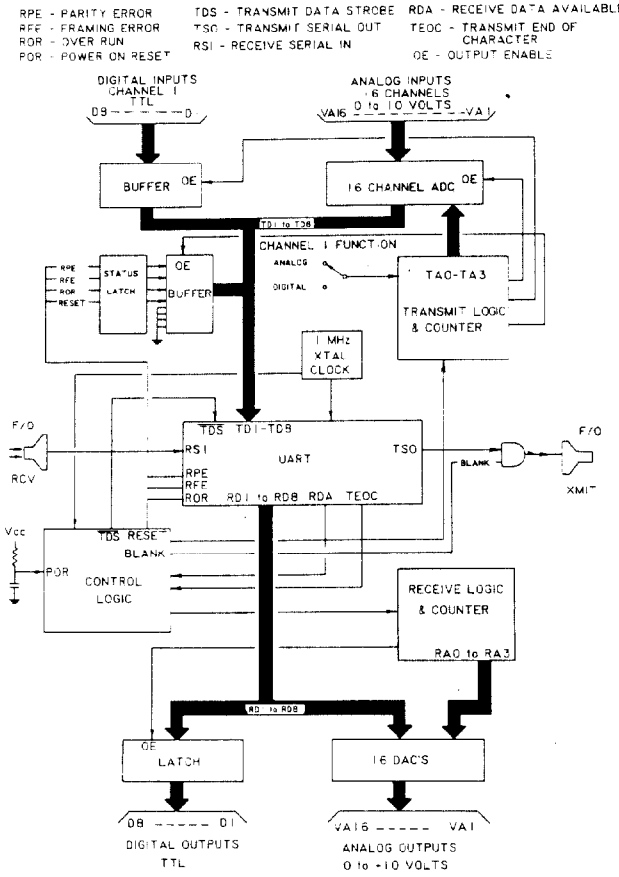

Figure 3. Block diagram of slave unit.

Figure 4 is a block diagram of the stand-alone master. On power up, the master goes into the reset mode where all DAC outputs are zero and zeros are transmitted on all channels sent to the slave. When the START command is received, the input data from the digital input or A/D converter is loaded into the UART and transmission is initiated. The input channel number is incremented and the cycle repeated up to the preset number of channels. If the master does not receive data from the slave, it will continue transmitting with all output data words set to zero. When the last channel is sent, the BLANK flag is set, the optical link is set to mark and the channel counter is reset. After three UART cycles, a new frame begins. A "link failure" flag that is set when the last channel is sent is cleared by a received data word. If it is not cleared by the end of a transmission frame, a link failure is considered to have occurred. After two link failures the master goes into the reset mode. The slave is synchronized to the master on receipt of the first data word from the master in both the reset and normal mode. It takes, at the most, two frame times for a link failure to cause a shutdown. At the end of a frame, the number of the last received channel is compared to the number of channels selected. If they are not equal, the "out of synchronization" flag is set. Other error flags are parity error, framing error and overrun, all derived from the UART. The master has an 8-bit data bus and 4-bit address bus to drive DAC's as well as a status output latch.

The modulus 16 output channel (address) counter is set to 15 by the BLANK flag. The first word received by the master is the slave status word which is sent to a latch where it is added to the master status word (latched from the previous cycle) for display. The next words increment the address counter and are latched, as appropriate off the board (usually by DAC's). There is also an interrupt line, which goes active if any error is detected.

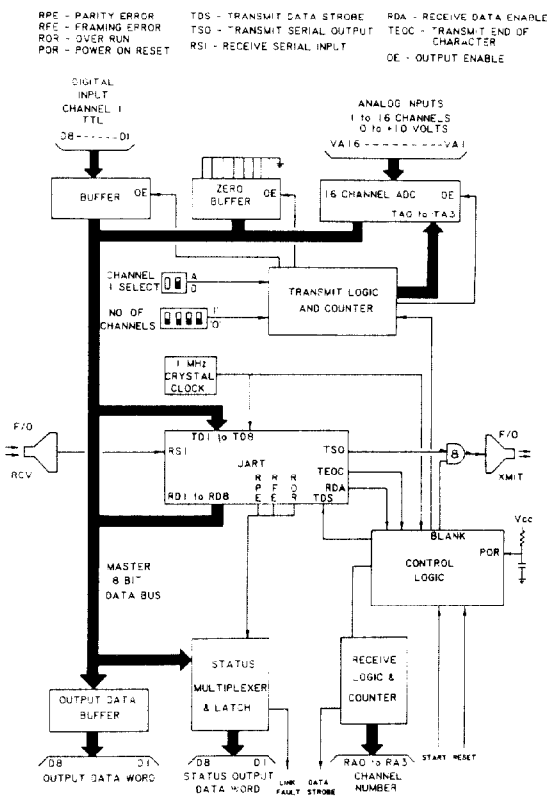

Figure 4. Block diagram of stand-alone master.

The UARTs are operated at their maximum clock frequency of 1 MHz. Since the UART requires 16 clock pulses per bit, the data rate is 62,500 baud. Each eight bit data word has added to it a parity bit, one start bit and two stop bits, giving a word rate of 5208 per second or a UART cycle time of 192 μs. Since each frame requires three extra UART cycles, one for the slave status word, one for synchronization and one for delays in data clocking in the slave; the frame rate for sixteen channels is 274 per second, and for 8 channels is 475 per second.

The master (Fig. 5), that is installed in the control computer, differs only slightly from the stand-alone unit described above. It appears to the central processor as sixteen input and sixteen output ports which access 32 bytes of on-board, dual port RAM. One output port controls the reset and start commands and the number of channels and one input port provides the status word. Fifteen data channels are provided, with the first channel as either digital (eight bits) or analog. The computer writes into a section of RAM the bytes to be sent to the slave and reads from the RAM the data sent from the slave. Automatic insertion of wait states prevents contention for memory. The data from the slave can also be sent to DAC's to control external equipment (as in closing the feedback loop for power supplies).

Wire-wrapped prototypes each fit on a 25 cm by 13 cm board. Hewlett-Packard series HFBR fibre-optic components are used because of their low cost, reliability, and ease of use. Cable length in excess of 20 metres is possible with these components at the relatively low data rate used.

The stand-alone master and slave are performing satisfactorily; the microcomputer master has not yet been tested in the field. This link provides low-cost, fast telemetry with good linearity and resolution (0.4%) for analog signals. The technique is scalable to additional channels of either analog or digital data.

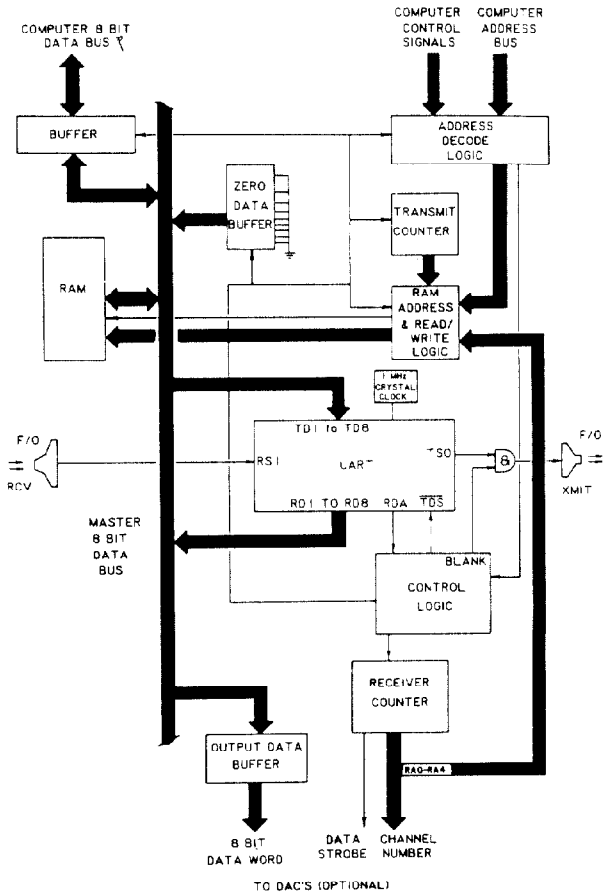

Figure 5. Block diagram of master for microcomputer system.

References

1. M. Amarandos, "Fiber-Optic Link Taps Time-Division Multiplexing", Electronics, December 29, 1982, p. 76.