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THE CERN SPS LOW BETA INSERTION CONTROL SYSTEM

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1. Summary

Within the context of the CERN SPS ppbar colliding beam experiments there are 2 x 15 power supplies which have to provide the currents necessary to produce the two low beta insertions. Their control system is described for both the hardware and the software parts. The references use a combination of an 18 bit DAC and an integrator to produce a relatively smooth drive signal to the current controlled power supplies. These 18 bit devices must operate in a hostile environment (electrical noises, temperature changes). Results are given on their performances, especially on the accuracy achieved at the required settings (better than 10^{-4} at intermediate levels) and, more important, the repeatability (of the order of 10^{-5}). Each set of 15 references is controlled from a dedicated computer. Each 60 msec point of each reference can be defined for a cycle length of up to 21.6 sec. The software driver is laid out such that during the pulsing mode (setting up) one can insert mini-coasts at any desired level or, during the coast proper at 270 GeV, one can adjust simultaneously the level of 1, some or all 30 references. The system also allows the setting up of a high beta in one insertion and a low beta in the other. It has transposed the theoretically calculated values so well that all the desired beta characteristics were achieved without having to add corrections due to inaccuracies in the reference control system.

2. The problem

Each power supply within a low beta insertion has a given influence on the beam which then defines the overall stability requirement. A first criterion established was that all power supplies would require unipolar reference control only. Another decision was to forego, if at all possible, a corrective feedback loop through DVMs and a computer.

This was based on the fact that a storage run is always preceded by a period of pulsed mode (with normally 14.4 sec repetition rate) and that high precision DVMs are essentially incapable of providing high precision results in areas where dV/dt is not equal to 0. This is especially true in the various round-offs. The appearance on the market of the first 18 bit DACs helped this decision. The reference design and philosophy for the Main Power Supplies would then be adapted to the new requirements, partly to save development time, partly because of its proven capabilities. The main parameters look as follows:

Max. output	:	10 V - 1 LSB
Resolution	:	> 16 bits, actually 18 bits
Speed	:	0 to 100% in < 0.5 sec
Accuracy	:	±2 x 10^{-4} of full scale
Repeatability	:	better than ±20 ppm
Polarity	:	unipolar
Output shape	:	smoothed

3. The reference (Fig. 1)

Each reference receives every 10 msec a 16 bit word indicating the change in amplitude during the following 10 msec. Of these 16 bits, 1 is held as a spare for future use, 1 serves as a reset bit, thus when desired, allowing to fix an absolute value in the digital summing unit preceding the digital/analog conversion module. Thus, 13 bits plus a sign bit are left for the amplitude information.

With these 13 bits, it is possible to reach full scale (18 bits) in (2↑5 + 1) x 10 msec = 330 msec considering the fact that one transmits 32 x (2↑13 - 1) bits. Thus the speed requirement was easily satisfied.

To achieve the smoothed output form, the voltage increment is applied to the integrator stage opposite to where the actual output is going. This provides some extra drive, the normal time constant R1xC1 being >> 10 msec. R2 must be adjusted appropriately.

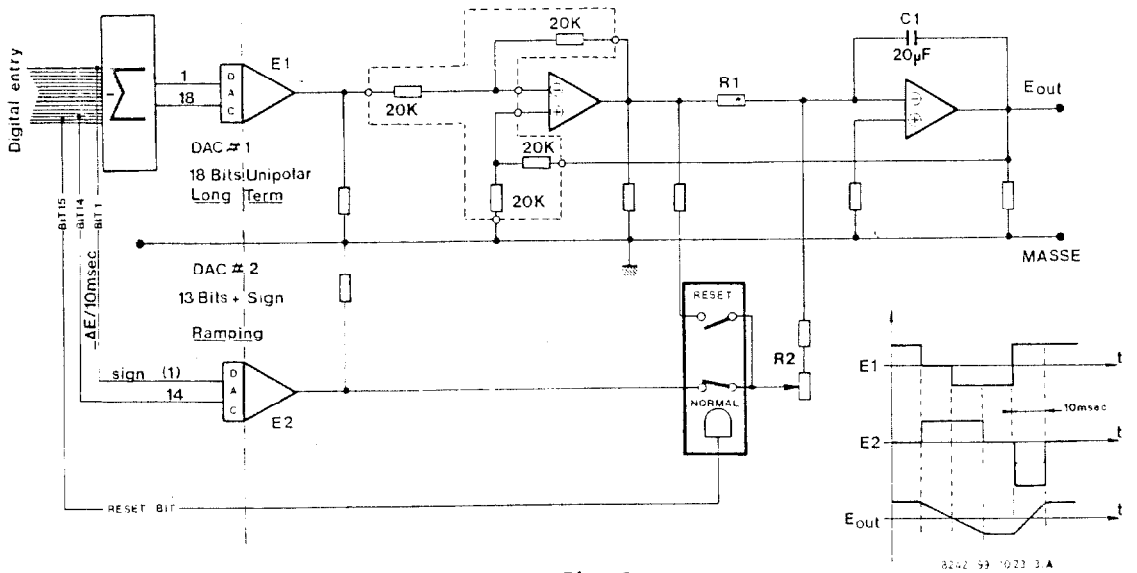

Fig. 1

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The transfer characteristic for a step input looks as follows:

$$E(OUT) = E1 \times (1 - E2x(R1/R2)) \times (1 - e^{-t/R1xC1})$$

for $0 < t < 0.01s$, where E1 is the increment DAC=1 and, as desired, at E_{OUT}, and E2 is equivalent to -32×E1.

R1 was chosen to be 2.61 kΩ, which results in R2 being about 18 kΩ. E1 then contributes approximately 17% to the change in output, DAC=2 contributing the remaining 83%.

Experience to date has shown that the reference as such has lived up to expectations. Linearity, repeatability and resolution proved to be better than expected, even though the units are housed in an industrial environment close to high power rectifier stations. Problems of accuracy were mainly caused by varying supply voltages from location to location, having initially calibrated the reference in the laboratory. However, rarely did it exceed 1 mV or 10^{-4} full scale. Adjustments in the field can be effected on Offset, Gain and Ramping.

4. Interface system for measurements

Even with a reference reproducing the desired curve shapes very closely during the pulsed mode, it is imperative to have monitoring facilities if only to be able to close an eventual loop. The loop becomes a necessity if the lags due to the current controlled power supplies should turn out to be detrimental to the beam optics. However, the DVMs must be centralized close to the controlling computer. Thus each current signal and also the reference signals must be fed back to this central location. The aim was to get these signals back with an accuracy of the order of $\pm 10^{-4}$. Two interface modules, each with differential inputs and independent power supplies within to handle the actual and the the inverted signal, were developed for this purpose. Low temperature coefficient resistor networks with two pairs matched to ±0.005% within and between the pairs, were used throughout. To reduce further pickup noise each input stage was followed with a stage containing a double roll-off (-40 dB/decade) with the -3 dB point at 300 Hz. However, as the distances to the 15 units are not equal and in order to keep all modules freely interchangeable, the differing d.c. resistances in the lines were not exactly matched. A final accuracy of $\pm 2 \times 10^{-4}$ rather than of $\pm 10^{-4}$ was achieved for the signals originating from the power supplies at the extreme locations.

5. The software

Each low-beta section has its own controlling computer which has three tasks: driving each of the 15 references every 10 msec, every 60 msec measuring one half of the 15 DCCT signals and, if asked to do so, calculating an improved cycle for a given system.

a) Reference driver/measurement

Each system can be turned on and off independently, and each has three tables. A first table defines the change in output for each 30 msec period. It was found that this is sufficient for a good cycle definition. Thus the driver must apportion this value to the three respective 10 msec segments. A second table contains the DVM measurements every 60 msec, three accesses per DVM being necessary. The DVMs work on a call basis to a CAMAC crate controller, each call being handled asynchronously. It was found that in this way the CPU load is more evenly distributed. A third table contains the theoretical (demanded) values every 60 msec. It is used only for correction purposes. The average CPU load without corrections on is only about 25%, some peak times going to 50%. The driver is built to handle also transmission errors. Earlier experience elsewhere however showed these to be so infrequent that they were never connected back to the appropriate CAMAC equipment. The driver naturally must do the formatting of the values, send off and check against curve shapes which may exceed the limits of 0 V downwards or 10 V upwards, at which level it simply clamps.

b) Corrections

The correction algorithm used is very simple. In order not to be dependent on any past situations only the slope of a given 60 msec period is compared to its demanded value and adjusted. This is done throughout the cycle with the exception of a 120 msec period in which an absolute value is set if it is in a pulsing mode. As also one absolute value must be fixed, the relevant measurement is done at T = 0 of the cycle and then the absolute value adjusted accordingly. Due to various choices made earlier, this level can be set with a 15 bit resolution only, but could however be extended to the full 18 bit resolution by changing and expanding the relevant software.

As the corrections are intended for correcting large initialization errors and errors due to power supply lag only, they run for 1 cycle at a time and must be restarted afterwards. The start of the corrections can be triggered by either a direct operator command or by a scheduled program on any given criteria.

The corrections cannot be turned on during a storage run as the trigger point lies outside the conditions existing in the storage mode. This is done intentionally as there are other means of changing levels at that time.

c) Command possibilities

The following is a non-exhaustive list of possibilities with the existing software.

- It is possible to insert in the injection and at the storage level of the pulsing mode any number of "coast" cycles on a repetitive basis. All active systems are affected. A common mode of operation during ppbar set-up is 1 cycle inserted at injection, none at the storage level, thus essentially doubling the SPS cycle.

- A single command will send all active units an operator-chosen number of coast cycles, i.e. into the storage mode. The same command will subsequently extend this mode. On the stop command the supplies will return to the pulsing mode synchronous to the CERN-PS.

- Each system has a small table where a change can be programmed. On a single command all these changes will again be applied synchronously. This is applicable in the coast mode only.

- The correction cycle can be started for each system independently or for all at once.

- Each system can be started/stopped individually. A single command allows all systems to start at the beginning of the next cycle.

d) Computer memory requirements

Each insertion is, as mentioned, controlled by its own computer. Provisions are made to accommodate 18 systems, i.e. function generators. Each system has its own table defining the output each 30 msec, a table listing the demanded value each 60 msec and a table listing the measured value each 60 msec. There is a general driver for the output and a dedicated driver for the 8 DMVs used.

The total space requirements in computer memory are then as follows:

- Data areas	:	52 K
- Output driver	:	2 K
- DVM driver	:	1 K
- Correction program	:	1 K
- General overhead	:	2 K
- Special Nodal functions	:	8 K
	ca.	66 K

The remainder of the computer space is taken up by the standard computer system used at the SPS.

6. Some results

One of the power supplies was selected for long-term stability measurements. One measurement per minute was made during any storage run longer than that interval. In Fig. 2 the points are plotted every 10 minutes, in Fig. 3 every 30 minutes.

Fig. 2

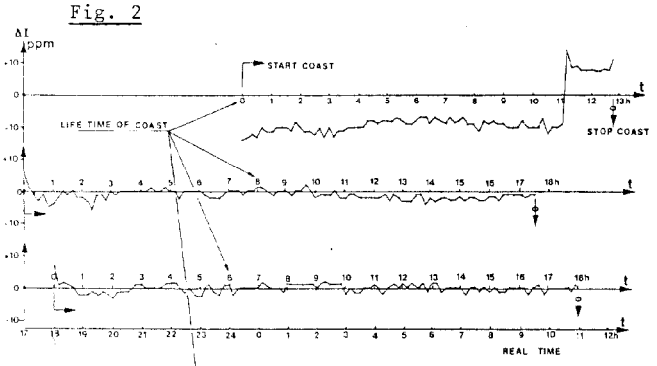
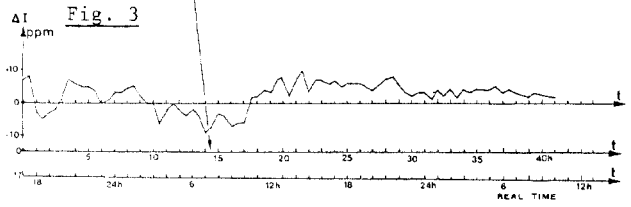


Fig. 3



7. Concluding remarks

A similar system has in the mean time been introduced into the control system of the SPS main power supplies. Experience during the start-up of 1983 of the CERN-SPS machine has shown that the repeatability of the described system has fully met the expectation. It has however also shown that the initial accuracy, when the whole machine is concerned and not only a part of a sextant as with the low beta insertion, is not sufficient. The lag introduced by the current controlled power supplies then kills the beam at the latest in the initial stages of acceleration. However, with the correction program applied during 3-5 cycles and subsequent trimming of the machine, it was shown that on a subsequent restart the machine would be right back in operational mode due to the excellent repeatability of the system.