

MICROPROCESSOR TECHNIQUES AND CONSTRUCTION AT THE NSLS*

J. D. Klein and J. F. Sheehan
National Synchrotron Light Source
Brookhaven National Laboratory, Upton, N.Y. 11973

Abstract

A description is given of the microprocessor systems in use at the NSLS,¹ which utilize Intel Multibus* and NSLS-developed printed circuit boards. Ease of manufacturing and flexibility of developing different systems from a set of NSLS standard components will be emphasized, and the low cost factors of each system and the utilization of off-the-shelf components will be indicated.

Introduction

The microprocessor systems developed at the NSLS for control functions utilize IEEE 796 Multibus and NSLS developed printed circuit boards. A concept was developed for ease of manufacturing and flexibility to satisfy the requirements of most systems. This was achieved by using a set of standardized components, that can be easily implemented into a specific microprocessor system, and be quickly assembled and debugged. The system type and hardware decisions were made so that a compromise between system cost and flexibility was achieved. Components are available from two hundred or more manufacturers of Multibus compatible equipment. In 1978 a survey was conducted to examine the available hardware for control systems for the NSLS. Many commercial process control systems were usually found to be limited to either communications distance, specialized application, single source of supply or of in-house manufacture. Basic considerations were:

1. Centralized computer versus distributed processors.
2. Communications speed versus cost and complexity.
3. Multiple sources of supply versus single sources or a custom "in house" system.
4. Existing "mature" technologies versus the delay and uncertainties of custom and state-of-the-art systems.
5. Flexibility of hardware packaging to cover the widespread range of environmental conditions and system size considerations.
6. Provisions for implementing entire feedback and control systems and not simply a data based setpoint and logging system.

While not any one system is the panacea for all process control, the introduction in the late 1970's of many small board level and packaged microprocessor systems has led to the production of many software and hardware packages with the flexibility to out perform the custom systems formerly used in the particle accelerator community. The extensive use of Camac and Nim in the accelerator field is common, but the majority of such equipment has been designed for experimental data collection rather than accelerator control. The GPIB and other similar buses are limited in scope and physical size.

The choice of multibus over other microprocessor based systems is reflected in its application at other accelerator facilities.²⁻⁹

The criteria for the NSLS system was for a packaging and microprocessor bus system rather than on a specific processor chip. The building blocks of most systems start with a NSLS developed chassis, industry standard power supplies and Multibus printed circuit board card cages. The basic microprocessor system contains two cards, an NSLS developed communications board and one of several available CPU boards. The communication card was developed to increase the speed of the serial computer link and contains added buffered interrupt and memory functions. Additional slots are available for memory boards or for many other varied uses. The Multibus is designed so that it can be expanded in modular increments. The chassis can accommodate 4 to 16 printed circuit boards. The system bus is often divided into two separate buses in order to break system grounds, where the second system it is often analog processing cards.

All accessory items are pre-made and contain all functions. The system is then assembled into its particular control function and the different types of systems are constructed from the basic microprocessor format.

Chassis Hardware

The chassis is a NSLS developed design and consists of a front panel power supply mounting plate, right or left side plate, rear panel or divider plate and a top or bottom cover. The sheet metal is designed so that four different pieces will make a complete chassis. All connections to the system are made on the rear panel and vary according to system application.

The front panel and power supply mounting plate is independently removable from the chassis. This gives access to the power supplies without having to remove the system from the control rack. The divider plate serves as an AC shield and mounting bracket for the printed circuit card cages. The side plates have holes for mounting cooling fans for ventilation. The back has all the external electrical connections mounted on it.

The electrical connections consist of an AC harness that provides power to the power supplies and fans, a communication harness that provides RS232, RS422, timing and reset control to the central computer system and the third harness is determined by the particular application of each system.

The processing system is housed in the first card cage and the slots are typically in the following order:

1. High speed communication board (NSLS Design)
2. Memory Board (System development)
3. Slave (open)
4. CPU board.

The second card cage contains printed circuit boards that interface to I/O equipment. The connections are made on the top of the board and follow a standard port configuration and are interconnected by mass terminated ribbon cable. The interface boards are both commercially available and NSLS developed. Typical I/O printed circuit boards are, differential or single

* Research supported by the U.S. Department of Energy.

ended input Analog to Digital converters, bit expansion I/O ports, optical isolation, 20 channel 16 bit timer boards, Ramp function controllers, video raster generators, interface boards to IEEE 488 and other standards, computer buffer and switching boards for allowing all serial lines to change computers without computer intervention.

Additional card cages can be either connected on the bus or operated as an independent system. When the cage is disconnected from the bus, the purpose is to break the ground connection. In the isolated mode the card cage has its own power supply and is connected to the rest of the system either differentially or optically. Both 12 bit and 16 bit analog servo cards are used in the NSLS system with all analog servo hardware being in the micro crate. The packaging of CPU, function generators and servo cards in a single enclosure allows control of precise programmed generation of magnet and R.F. functions at megahertz rates without central computer intervention.

Another I/O interface is use of industry standard optical isolator boards such as PB-8,16,24, family which are made by many different manufacturers. These give direct interface with the equipment and conforms to the I/O port configuration. Some of the common types of microprocessor systems used at the NSLS are:

1. 16 channel integrating power supplies.¹⁰
2. Ramping function power supply.
3. Vacuum pump control.
4. Kicker timing and reference control.
5. Machine timing.
6. Central computer interfaces.
7. Operator consoles and displays.

Many special purpose "one of a kind" systems are used but incorporate much of the standard hardware and software that is used in other systems. The photos below show the chassis components and a completed microprocessor system.

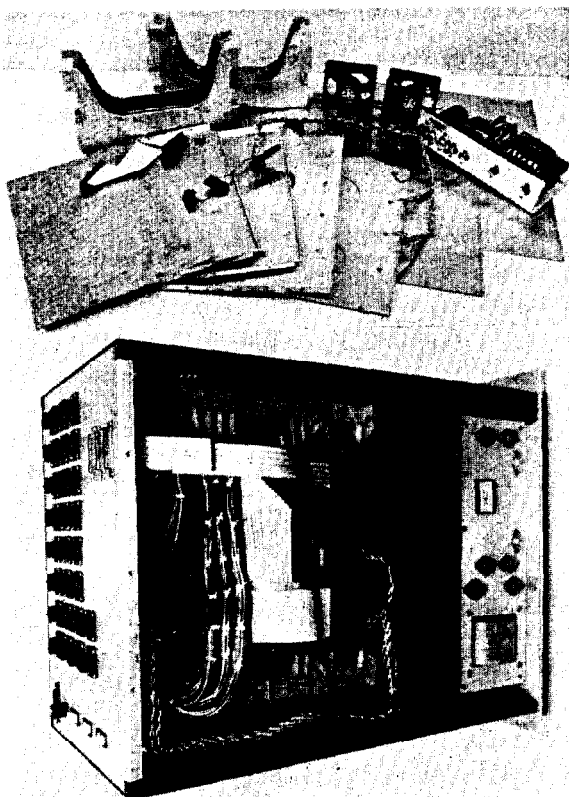


Fig. 1.

System software and hardware development is performed on the target system eliminating the problems of emulators and the subtle bugs that can occur in transferring from a development system to a different hardware unit.

High speed relocatable assembly code is generated on the NSLS central computer system. This gives the convenience of sharing the library features and storage and peripheral functions of a large central computer system with the ease of down loading the test routines or final code into the target system. Code can be operated from a system RAM or burned into EPROM with a standard EPROM programming card available for any of the systems.

System Checkout

Each microprocessor system is connected to the central computer by a twelve pair shielded (Datalene*) cable to allow RS422/423, RS232 and differential timing circuits.

All central communication, real time interrupts and system downloading is via this link. Unused pairs may be used for remote system reset or any custom function. Real time triggering of beam transfer equipment via these links is accomplished with a trigger jitter of less than one nanosecond.

System Reliability

Initial operation of the microprocessor systems required the computer being located about one mile from the microprocessor systems with the data line being composed of both underground burial and overhead lines. Occasional lightning storms resulted in destruction of many driver/receiver integrated circuits on several lines. The addition of Transorb* voltage limiters and elimination of the long cable run has reduced the problem but not totally eliminated it. Occasional memory chip failures and failures of optocouplers because of degraded forward gain have occurred as symptomatic early life failures. The failure rate from all causes is small enough that they are not presently recorded. The ability of the systems to tolerate high environmental electro magnetic noise, and occasional short power dropouts exceeds that of any of the power supply equipment or building services.

Summary

A microprocessor based control system for a custom application can easily be produced from a group of standardized components in a Multibus configuration. The assembly can take as little as an hour to six hours for a complex system. The cost effectiveness is realized due to labor saving, inexpensive connections, off the shelf components and NSLS developed hardware. The cost of a chassis minus the printed circuit cards is an approximate average of six hundred dollars.

The ease in testing the system is achieved by the NSLS monitor in EPROM and test programs in the central computer system.

* Multibus is a Trademark of INTEL Corp.

* Datalene is a Trademark of the Belden Corp.

* Transorb is a Trademark of General Semiconductor Industries, Inc.

References

1. K. Batchelor, B. B. Culwick, J. Goldstick, J. Sheehan, J. Smith, Distributed Control System for the National Synchrotron Light Source, Proc. of the 1979 Part. Accel. Conf. IEEE Trans. Nucl. Sci. NS-26 No 3 p 3387.
2. H. D. Lancaster, S. B. Magyary, J. Glatz, F. B. Selpha, M. P. Fahmie, A. L. Ritchie, S. R. Keith, G. R. Stoner, and L. J. Besse, A Microcomputer Control System for the Superhilac Third Injector, Proc. of the 1979 Linear Accel. Conf. Montauk, N.Y., pp 269-273 (BNL-51134).
3. R. W. Goodwin and M. F. Shea, A Distributed Linac Control System Featuring SDLC Loop Communication Proc. of the 1979 Linear Accel. Conf. Montauk, N.Y. pp 274-278 (BNL-51134).
4. E. R. Martin, C. M. Schneider, V. A. Martinez, R. E. Trout, and R. E. Gritz, Evolution of the Racetrack Microtron Control System, Proc. of the 1981 Linear Accel. Conf. Santa Fe, N.M. pp 171-173.
5. R. W. Goodwin and M. F. Shea, The Distributed Control System for the Fermilab 200 MeV Linac, Proc. of the 1981 Linear Accel. Conf. Santa Fe, N. M. pp 277-280.
6. R. Melen, A New Generation Control System at SLAC, Proc. of the 1981 Part. Accel. Conf. IEEE Trans. Nucl. Sci. NS-28, No. 2 Part 1 p 2142.
7. E. Bozoki, B. B. Culwick, and J. D. Smith, Status of the National Synchrotron Light Source Control System, Proc. of the 1981 Part. Accel. Conf. IEEE Trans. Nucl. Sci. NS-28, No. 3, Part 1 p 2183.
8. S. Magyary, H. Lancaster, F. Selph, M. Fahmie, C. Timossi, J. Glatz, A. Ritchie, J. Hinkson, R. Benjegerdes, D. Brodzik, Operating Experience with a New Accelerator Control System Based upon Microprocessors, Proc. of the 1981 Part. Accel. Conf. IEEE Trans. Nucl. Sci. NS-28, No. 3, Part 1 p 2201.
9. Walter S. Trzeciak, Aladdin Computer Control System, Proc. of the 1981 Part. Accel. Conf. IEEE Trans. Nucl. Sci., NS-28, No. 3, Part 1, p 2273.
10. J. Sheehan, H. Langenbach, Power Supply Regulation by Microprocessor, IEEE Trans. Nucl. Sci. 1983 Particle Accelerator Conference.