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FASTBUS FOR DATA ACQUISITION AND CONTROL*

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Summary

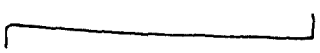
FASTBUS is a standardized modular data-bus system for data acquisition, data processing and control applications. It is the result of an interlaboratory development undertaken to meet the needs of the high energy physics community. However, the versatility, speed and addressing capability of FASTBUS make it attractive for many other types of application.

A FASTBUS system consists of bus Segments which operate independently but dynamically link together as needed for operation passing. This parallel processing feature accounts to a great extent for the high throughput of FASTBUS in multisegment systems. Master modules compete for single or multiple Segment Control through a bus arbitration scheme using assigned priorities. Logical, geographical, secondary and broadcast addressing methods are used to access either data space or control and status register space. Features include block transfers, a sparse data scan and interrupts.

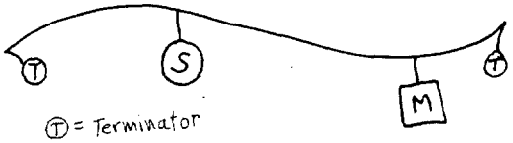
Segments

A FASTBUS Segment is a bus that operates autonomously but that can also be part of a larger bus system containing other Segments with which it communicates. The Segment includes 32 lines, used for both addressing and transmission of data. In addition there are lines for control, timing and information, as well as for distribution of power to FASTBUS Modules.

There are two types of Segments; Crate Segments and Cable Segments. The Crate Segment is mounted at the rear of a FASTBUS Crate where it can be accessed by a multiplicity of Modules housed in the Crate. Here is the symbolic representation of a Crate Segment with the bus lines terminated at both ends.

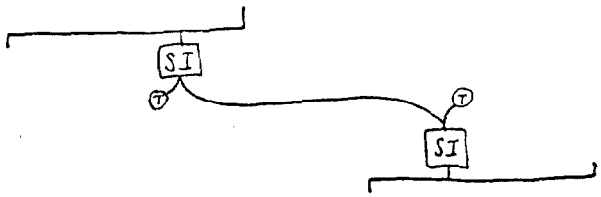


A FASTBUS Cable Segment consists of a cable together with connectors for mating with FASTBUS Devices. Here is a terminated Cable Segment with attached FASTBUS Slave (S) and Master (M) Devices.

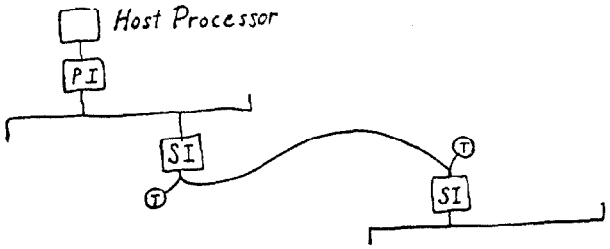


System Topology

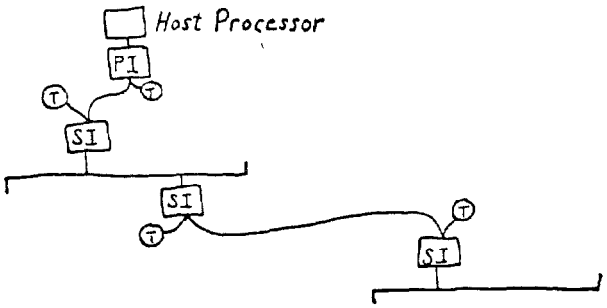
We interconnect Crate Segments through Segment Interconnects (SIs) and Cable Segments as here -



To link a Segment to a host processor (usually a computer) we use a processor interface (PI) that can be a FASTBUS Module and connect it as shown -



or we can have the processor interface independent of the Segment and possibly physically located with the processor or otherwise remote from the Segment. We then interpose a Cable Segment with Segment Interconnects between the Segments and the processor -



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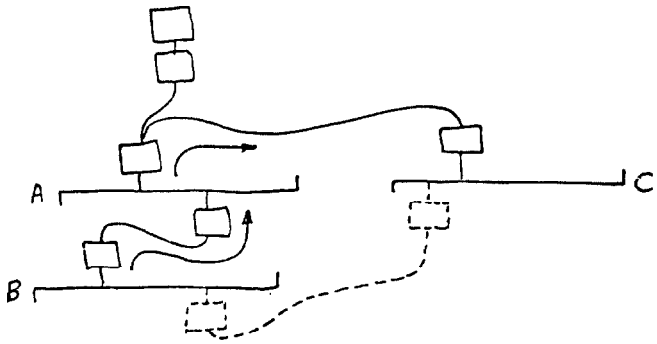
Let's add a third Crate Segment -

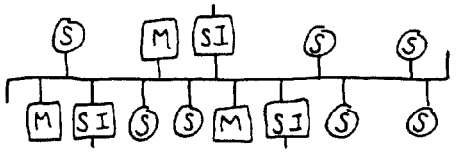


With the solid line connections shown, traffic between Segments B and C follows the solid arrows and passes through Segment A. Segment A's ability to provide service to its family of Modules is affected by the amount of traffic between Segments B and C. As this traffic increases, service to Segment A's Modules is degraded. If the degradation can not be tolerated we can provide an alternate route for B-C traffic by linking B and C directly through SIs as shown by the dashed lines. In general we can connect Segments as a simple parallel system, in a tree structure, or in any combination, with cross connections as needed to optimize the transmission paths.

We will recognize that Segment Interconnects must be sophisticated devices to perform their tasks of linking Segments, selecting routing paths and transmitting addresses and data.

Master and Slave Modules

Master Modules (M) and Slave Modules (S) are the workhorses of a FASTBUS system. As the names imply, Masters can acquire control of the Segment and initiate operations whereas the Slaves are simple souls that can only take their instructions from the Masters. Here's a Crate Segment with its Slaves and Masters and a few Segment Interconnects -



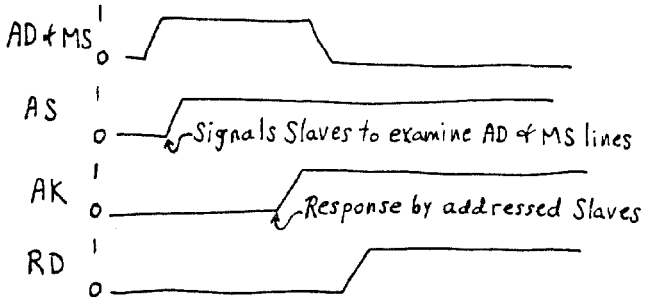
Addressing

A Master initiates a FASTBUS operation by addressing the Slave (which may be a Master acting as a Slave) with which it wishes to communicate. This procedure is designated a "Primary Address Cycle." Since Primary addressing involves writing to the addressed Module, the Read (RD) line is maintained at a logical zero. Mode Select (MS) lines specify the type of address. Here are the MS assignments (they'll make more sense a little later) -

MS Encoding for Address Cycles	Address Type
0	Specific Device - Data Space
1	" " - CSR Space
2	Broadcast - Data Space
3	" - CSR Space
4,5	Reserved - Specific Device
6,7	" - Broadcast

Now let's have a Master address a Module by keeping the Read line at zero, asserting the Mode Select lines as appropriate, and gating the desired address onto the Address/Data (AD) lines. The Master then pauses before asserting a synchronizing signal, Address Synch, (AS) in order to allow the AD lines to settle before the Slaves inspect their contents.

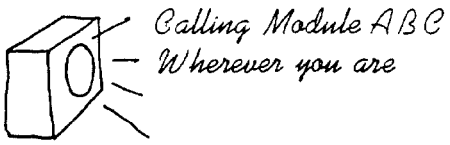
Upon recognizing its address on the AD lines, a Slave responds by asserting the Address Acknowledge (AK) line. Here's the way it looks as time marches to the right -



For the remainder of the operation AS and AK remain asserted, constituting the AS/AK lock. So long as this lock is maintained (and it can be broken only by the Master), the Master-Slave communication path is inviolate and the Master and its Slave have exclusive use of the bus. Thus, after receiving the Slave's Address Acknowledge, the Master is safe in clearing the address from the AD lines and can then use them for transmission of data. RD is held at logical zero for Write data and at logical one for Read data. Addressing modes include Logical, Geographical, Broadcast and Secondary. Except for Secondry Address, they are all asserted during Primary Address Cycles.

Logical Address

A Device is assigned a Logical Address of 32 bits consisting of the Device Address and an Internal Address (internal to the Device). The Device Address in turn consists of the Group Address, which identifies the Segment on which the addressed Device resides, and the Module Address which selects a particular Module on the Segment. Each Device capable of being logically addressed contains a Device Address register which is fully accessible by standard FASTBUS operations and which must be initialized by the system start-up procedure.



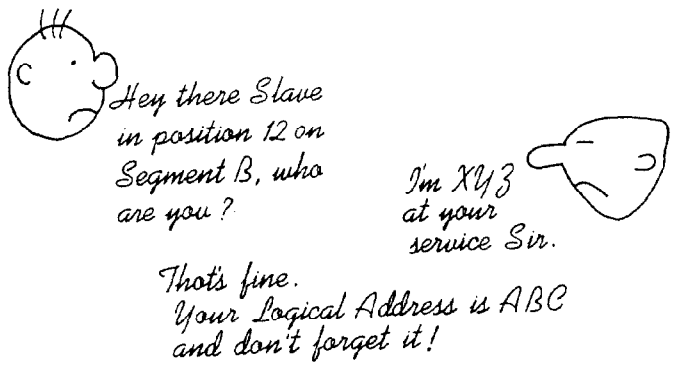
During a Primary Address Cycle in which a Logical Address is specified Slaves that have been enabled for logical addressing compare their Device address register content with the address on the AD lines. The Slave that finds a match then returns Address Acknowledge and the operation continues as described above.

Geographical Address

The Geographical Address of a Device is a Primary Address based on the physical (geographical) location of the Module on a Segment. It is specified by coded backplane pins (GA pins) on a Crate Segment and by switches on a Cable Segment.

In Geographical Addressing a Geographical Enable line is asserted and the Geographical Address of the desired Module is placed on the AD lines. When a Slave detects a match between the contents of the AD lines and the coding of its GA pins, it recognizes that it is being addressed and therefore attaches to the bus and the operation continues as described above. A Master on one Segment can Geographically Address a Slave on another Segment provided the Master knows the Slave's Group Address.

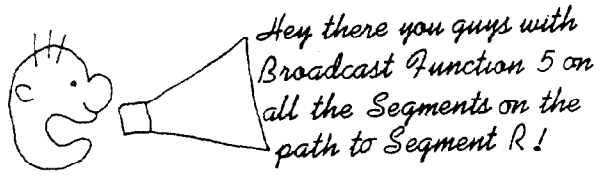
Geographical Addressing is the one addressing technique that is mandatory for all FASTBUS Modules. It must be used during system initialization to read and write registers such as the Device Identification register and the Device Address register.



But that's just one implementation of Geographical Addressing. It can also be used in conjunction with Secondary Address Data Cycles for general addressing in lieu of Logical Addressing.

Broadcast

A Broadcast is an operation in which a Master attaches simultaneously to more than one Slave during a Primary Address Cycle. It is useful for various purposes such as synchronizing Device actions or clearing a bank of counters. Broadcast Addressing is via the AD lines with appropriate coding of the Mode Select lines. Since more than one Slave and frequently more than one Segment is involved, a Slave Acknowledgement is not meaningful and a "System Handshake" from ancillary logic is needed to assure the Master that the Broadcast has propogated to all addressed Devices before the Master initiates data transfers.

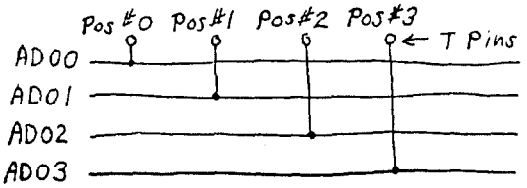


Secondary Address

In addition to the 32 bit-wide address space available to an entire system, an expanded address space is possible within each Device. After having been selected by a Primary Address Cycle further address information can be sent to the Device as data during a Secondary Address Cycle. Since the address is transmitted in a Data Cycle, you do not see an Address Cycle MS Code for it. But be patient, you will soon note a Data Cycle MS code for a Secondary Address.

Sparse Data Scan

In many experiments only a small fraction of the Devices that can accept data from detectors actually acquire data during an event. The Sparse Data Scan of FASTBUS is a mechanism that allows the rapid location of these Devices. It makes use of an unbussed pin (T pin) which is at each Device position on the Crate Segment. The T pin at position n is connected to AD line n thus -



A Master wishing to start a Sparse Data Scan issues a Broadcast command to all appropriate Devices on a Segment asking those with data to respond on their T pins. A read of the AD lines then indicates which Devices should be interrogated for data. This capability can be provided on a Cable Segment by using patch pins or switches.

Data Cycles

In terminating the Address Cycle the Master removes the address information from the AD lines. The Master can then begin a Write Data Cycle by asserting the data on the AD lines together with Data Synch (DS), RD=0, and the appropriate MS code. The Slave responds with a Data Acknowledge (DK) indicating that is has received data from the Master. To obtain data from a Slave the Master asserts the Read (RD) line and the Data Synch line as well as the appropriate MS code. The Slave responds with Data Acknowledge, telling the Master that the data is on the lines.

The operation is terminated by the Master removing all its signals (including AS) from the bus. The AS=0 information reaches the Slave, after traveling down the bus, whereupon the Slave removes all of its signals.

Here are the Data Cycle MS codes -

MS (encoded value)	Interpretation
0	Random Data
1	Block Transfer - Handshake
2	Secondary Address
3	Pipelined Transfer (Non-Handshake)
4-6	Reserved - Handshake
7	Reserved - Pipelined

(Now you've spotted the MS code for a Secondary Address which, as mentinoned earlier, is transmitted in a Data Cycle, not in an Address Cycle.)

Block and Pipelined Transfers

A block transfer consists of an Address Cycle followed by a number of Data Cycles of the same type, that is, all Read or all Write. The connection between Master and Slave is handled as described above with full handshake at the begining and end of an operation. Speed is enhanced by using both transitions of the Data Synch and Data Acknowledge signal pair while still providing full handshake protection for the data transfers.

Pipelined transfers (block transfers without handshake) can be used between Devices that can handle the same data rates. However the time saving, as compared with full handshaked operaton, is usually slight and it is generally better to use the more reliable handshake mode.

Responses

FASTBUS includes three Slave Status (SS) lines which, like the MS lines, have different meanings for Address and Data Cycles. For Address Cycles they indicate to the Master whether the requested connection was made and if not, the reason for the failure. For Data Cycles information concerning the availability of the Device (busy, full or empty) and validity of a Secondary Address or data is conveyed. The SS data response also makes clear if the Device has accepted or supplied data.

Control and Status Register (CSR) Space

If we back up to the table showing MS code for Address Cycles we see that, depending on the MS coding, one can access normal Data Space or CSR (Control and Status Register) Space. The CSR Space, as distinct from Data Space, is provided since certain registers and functions in Devices need to be separated from the normal data registers in a way that provides some protection from accidental access while not interfering with the allocation of addresses to the normal data portions of the Device. For example, two memory Devices should be able to have their contents accessible as a single larger memory. However, they may each contain control registers and status registers associated with memory protection or error detection and correction, and these registers must also be accessible. Furthermore, it is desirable that Devices have basic status and information registers in standard locations so that they can be readily accessed by standard shared programs.

This is accomplished in FASTBUS by selecting Control and Status Register (CSR) Space in a Primary Address Cycle followed by a Secondary Address Cycle to select a register in CSR Space, and a Data Cycle to transfer data to or from the register. Addresses of and bit positions within CSR registers are specified for the usual control functions and status indications. A large region of CSR space is available for user specification.

Arbitration for Mastership

When more than one Master wants control of the bus at a given time, a decision must be made as to who gets Mastership. In FASTBUS the decision is made by the competing Masters themselves during an Arbitration Cycle, utilizing preassigned priorities (Arbitration Levels) stored in Arbitration Level registers within the Masters. An Arbitration Cycle does not interfere with other activity on the bus hence the next Master can usually be selected before the current Master has completed its operation.

The Arbitration Cycle is controlled by an Arbitration Timing Controller (ATC) that monitors an Arbitration Request line for requests from Masters applying for Mastership. The ATC supervises and times the Arbitration Cycle in conjunction with timing and control lines, operating under the constraint that the current Master need not permit an Arbitration Cycle until it is willing to do so. During the Arbitration Cycle the competing Masters play a variation of a game of six card stud by gating their Arbitration Level (priority) bits onto the six Arbitration Level (AL) lines and making a bit by bit comparison (starting with the most significant bit) between the contents of the AL lines and their own corresponding Arbitration Level bits. In this comparison, once a Master detects a logical one on an AL line while he has only a zero, he recognizes that he has been outprioritized, concedes defeat, and drops out of the competition. The process continues for all of the vying Masters until only the winner remains. The ATC, by lowering the "Arbitration Grant" line when the bus is free, then offers Mastership to the pending Master which returns a "Grant Acknowledge" to confirm that it accepts the offer.

FASTBUS has two classes of Arbitration Level, Local and System. The Local Level applies only to the Segment on which the Master resides whereas the System Level applies over the entire system. System Levels are all of higher priority than Local Levels.

A Master that has a heavy work load and that has been assigned a high priority could continually win arbitration contests thus denying other Masters an opportunity to gain control of the bus. Such a Master can be generous, at its option, and operate in the "Assured Access" mode whereby, after completing an operation, the Master refrains from participating in further arbitrations until the requests of all other Masters waiting for the bus have been satisfied. The problem of bus hogging can also be alleviated by assigning high priorities to the low duty Devices.

Interrupts

A FASTBUS interrupt is a request from a Device for service or attention. The interrupting Device addresses an interrupt sensing control register region in a processor and writes its own address and possibly other information concerning the reason for the interrupt into the registers. This provides the processor with the information it requires to access and service the Device.

In some systems many simple Devices may lack the capability of gaining bus mastership and performing an interrupt write operation. Such Devices may assert a Service Request (SR) line which can be monitored by a special Service Request Handling Device that can gain mastership and locate the requester. Special Broadcast operations make this procedure quite efficient. The Service Handling Device may then service the request or it may send an interrupt message on behalf of the requester to some other processor.

Logic Type

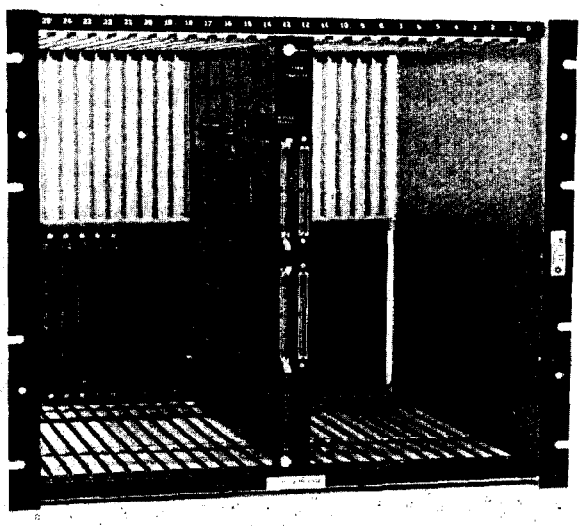
Current implementations of FASTBUS utilize ECL (Emitter Coupled Logic) for the bus because of its high speed capability. Within the Modules themselves, the designers are free to use any logic family that they may desire (TTL, MOS, etc.) except that at the Module-Bus interface the logic must be consistent with that of the bus.

Bus Speed

Though FASTBUS is a high speed system, it is difficult to state its speed in numerical terms since it depends on the type of logic devices, bus length (particularly for intersegment communications), type of operation and number of transfers involved and many other factors. With an ECL bus, an operation consisting of a Primary Address Cycle followed by a single asynchronous data transfer between a Master and Slave on the same Crate Segment, would require roughly 100 nanoseconds. To best realize the speed potential of the system it should be configured so as to maximize the intrasegment operations as compared to the intersegment.

Module and Crate Implementation

The photograph in this article shows a typical FASTBUS Module in a typical FASTBUS Crate that can house 26 single width Modules or a lesser number of Modules of multiple width. The backplane that constitutes the Crate Segment is seen at the rear of the Crate.



Information and Specification Availability

FASTBUS information and specifications are available from Louis Costrell, Chairman NIM Committee, National Bureau of Standards, Washington, D.C. 20234.