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# THE ENERGY SAVER/DOUBLER QUENCH PROTECTION MONITOR SYSTEM

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## Summary

The microprocessor based system to detect quenches in the superconducting magnets is described. Tests conducted over the past two years using a string of twenty superconducting magnets have yielded results having major impact on the design of this system. A network of twenty-four 16-bit microprocessors will monitor the integrated voltage across magnet protection units every 60 Hz line period using isolated voltage to frequency converters. These measurements are compared with the inductive voltage expected. Under transient conditions, the distributed L-C nature of the magnets delays signal propagation as in a transmission line. To achieve the required sensitivity of resistive voltage detection, the inductive voltage for each magnet cell is calculated using two of the six measured dI/dt signals. Prevention of faults to the magnet system by the monitoring connections, minimization of cabling, and matched transient response of all monitoring channels have been considered together in design of the hardware and software.

## Introduction

Plans for the Energy Doubler quench protection system have been described earlier.[1] Significant changes have been made in the system configuration and the quench protection monitor (QPM) design. An alternating coil-bus structure in two circuits has replaced the original plan having all the magnet coils in one loop with a second loop formed by the return bus conductor of all the magnets. A segment of the new circuit representing one lattice cell is shown in figure 1.

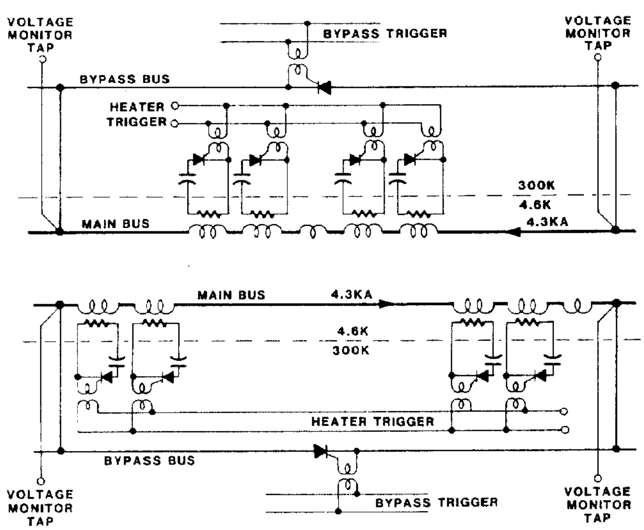


Figure 1. Quench Protection Unit

This new connection scheme removes the very difficult task of protecting the global return bus loop, removes a strong transient coupling between protection units due to the bus energy dumping, and removes a transient force on all magnets that would occur during every quench. It necessitates having two styles of bending magnets differing in their external connection detail and defines a quench protection unit to be a complete cell rather than a half-cell.

## Distributed Microprocessor System

The system must monitor a 6.3 km long ring of superconducting magnets. A single processor system would have an enormous cabling cost. This cost can be drastically reduced by distributing many inexpensive processors around the ring. Twenty-four processors were chosen not only because this number balances cabling and processor costs, but it also corresponds to the cryogenic and general utility grouping of the accelerator. An added benefit of more processors is a reduction in the number of channels each microprocessor monitors, allowing for more sophisticated attention to the protection of each channel in the same time period. The system is shown schematically in figure 2.

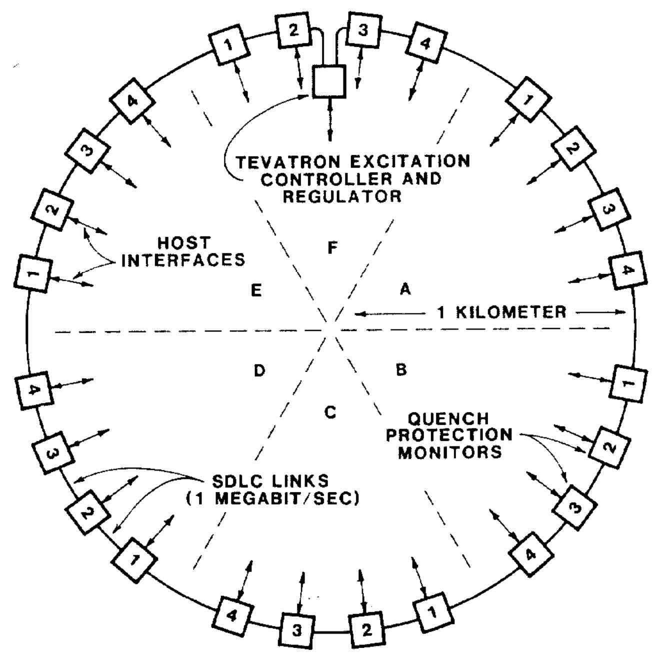


Figure 2. Distributed Microprocessor System

Primarily, each monitor autonomously protects its own section of the ring; in addition, the monitors are loosely coupled to each other in real time by an SDLC link.[2] This provides a more coordinated and versatile fault response on a global basis, and also provides real time parameter distribution for such auxiliary tasks as magnet excitation control. This link is multiplexed on the same cable that distributes analog information about the magnet current measured at six different places around the ring. An additional "hard wire" cable is used for backup fail safe fault response.

The primary protection task involves a precise analytic comparison between the expected magnet voltage and the actual measured voltage. The sensitivity and/or reliability of this comparison can be increased by taking into account higher order effects. The MC68000 16-bit $\mu$P was chosen for its strong real time analytic capacity.

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## System Test Experience

Three versions of prototype monitors have been constructed and tested, with a fourth version presently under construction. The first version served to test basic protection concepts. The second version included a commercial Z80 CPU, memory and I/O card and was housed in a NIM module.[1] An MADC was contained in a separate NIM module for data acquisition of magnet currents, voltages, etc. This prototype was operated at the test facility with a 4 magnet string and at full magnet current with only the heater firing unit (HFU) subsystem. In this test the magnets dissipated their internal magnetic energy without incident.

The third version of the QPM was radically different from the previous systems in a number of ways. To provide greater flexibility in the configuration of the monitor during the development phase, the monitor utilized an 8-slot MULTIBUS chassis. Commercial Z80 CPU and memory cards, and locally designed control and scaler cards comprised this system. Data acquisition occurred via 250 kHz voltage to frequency converters (VFC) and an 18-channel, 16-bit scaler card. A control card communicated control and status information between the QPM and critical protection subsystems such as the HFU, energy dump, quench bypass switches and power supply controls. This version of the monitor performed quite well with a 20 magnet string at the test facility, attaining a final quench detection sensitivity of approximately 3 volts.

Occasionally spurious quenching was induced by response mismatches in the voltage to frequency converters. This was corrected through transient response compensation in hardware and software. Spurious quenching also occurred due to jitter in the 60 Hz data acquisition period, resulting in miscalculation of the resistive voltage. In no instances, however, did the monitor system fail to take safe action when a real quench was detected or a problem with the monitor occurred.

All tests to this point have used the older global bus connection of the magnet string. A new test string configured with the alternating coil-bus connection is in the commissioning stage.

## Transient Propagation

The 774 dipoles and 240 quadrupoles are all connected in series electrically. The magnet coils in addition to their inductance have a significant capacitance to their surrounding cryostats which are grounded. The associated transmission line properties have been studied for the purpose of identifying and damping standing wave patterns that would interfere with the accelerated beam.3 The magnet circuit has been characterized as having an impedance of 600 ohms and a propagation velocity of 25 dipoles per millisecond.

This behavior is important to the quench monitor because the quench detection is based on comparing the voltage measured across a magnet cell with that expected by measuring dI/dt at some location in the circuit, that is,

$$V_r = V_{cell} - L_{cell} \frac{dI}{dt}$$

Since a voltage transient occuring at some location in the long series circuit has a slow propagation velocity, the dI/dt measured at another location in the circuit during the transient settling time will not result in a cancellation of the voltage measured across a particular cell. To keep the error contributed to the calculation of Vr by this phenomenon below the 0.5 volt threshold at which we need to operate, a combination of dI/dt signals obtained on both sides of any voltage monitor must be used. The sensitivity for detecting slowly growing quenches in the superconductor can also be enhanced by using a threshold which is high for short term signals and lowered for longer term integrated comparisons.

Current will be measured by transductors at the six warm-bus locations in the ring where the magnet circuit is brought out of the cryostats to power supplies. The I signal is differentiated in an analog circuit, this dI/dt signal converted to a pulse train, and fed into a serial data link connecting the QPM's together.[4]

As indicated in figure 1, voltage taps are provided at the boundaries between cells of the magnet circuit. These voltages are transmitted through isolation resistors and equal length cables to 1 MHz VFC's located in the service buildings. To allow a low quench detection threshold under transient conditions, the time constant (19.4 ms) of the roll-off due to the isolation resistance and the cable capacitance must be matched for all channels by cutting the cable lengths to a specific measured capacitance.

## Software

If a quench occurs, it must be detected before damage can occur in the superconductor. Quench protection is, therefore, a high priority 60 Hz interrupt driven foreground task programmed in assembly language. All analog measurements are integrated over one line cycle to exactly cancel power line harmonics and improve noise immunity. The protection task uses these integrated values to determine the state of all superconductors. A high impedance voltage sensing network is used to measure magnet voltage. This network affords fault isolation, but introduces space and time dependent distortions. These distortions must be removed, by a real time circuit model, before the true magnet voltage can be ascertained. In addition, transmission line effects around the ring must be taken into account before a comparison of magnet current ramp rate, magnet inductance, and actual measured voltage can be made. If a resistive voltage greater than 0.5 V is detected, the monitor shuts down the entire system and fires heaters in the quenched magnet protection cell, and allows SCR's to by-pass current around the quenched cell.

Control of critical protection hardware, like the heaters, is accomplished through a special 300 Hz interrupt driven activity. This heartbeat activity is constantly gathering status and controlling the critical hardware. If this activity should fail for any reason, the hardware will automatically default to protect the magnets as if each were quenching.

The background task handles data communications with the main accelerator control system and provides a limited status display and command processor for in-situ hardware evaluation.

To facilitate control system communications with a number of accelerator subsystems, including the QPM, a protocol has been developed which standardizes source and destination datum addressing. The protocol defines a transmission header which contains message source, destination, length and nature indicators. Both sequential and random access are provided.

All transmissions are initiated by the control system with either a read or set data command. Control system commands may originate in the central host computer or the local operator interface microcomputer. The host computer is responsible for setting up initial protection parameters, analyzing statistics to improve detection sensitivity, and collecting and interpreting the QPM quench event history data. The local operator interface provides QPM status display and limited parameter modification.

All set data commands are processed by a filter routine which checks incoming parameters against, and limits them to preset valid ranges. The processed output of the filter routine may be directed to a holding buffer or placed directly into the active foreground data base. Commands are provided to restore, read, set, and activate the holding buffer as well as read and set the active foreground data base. Critical data directed to the holding buffer may be subsequently read back and verified before being activated.

## Microprocessor Hardware

The present system is shown in figure 3.

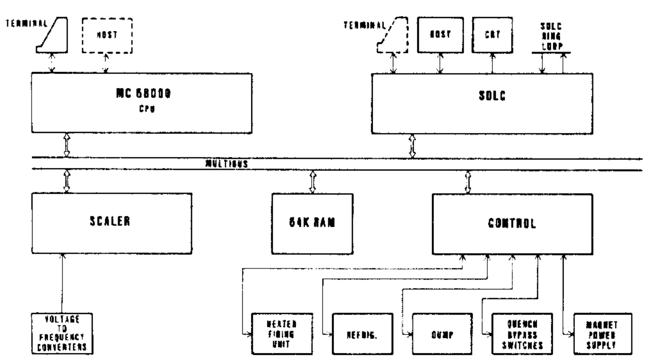


Figure 3. Quench Protection Monitor Block Diagram

All monitor hardware is housed in a commercial 8-card MULTIBUS chassis with a modified rear panel which folds back for ease of card removal. Rear panel connections are made with connectors which allow mass termination of ribbon cables. A transformer tap inside the chassis provides a signal for the 60 Hz interrupt generator.

An in-house MC68000 CPU card replaces the less powerful Z80 based cards found in previous QPM versions.[5] It includes two standard RS-232 connections for a data terminal and a serial link to a host computer. A 3-channel system timing module is used to generate the 300 Hz interrupt required for operation in critical protection subsystems. Up to 64 Kbytes of on board memory space (RAM and ROM) is provided. An SDLC card is included for communication between QPM's. External memory consists of a commercial 64 Kbyte RAM card to be used as an event data retention buffer.

A card with forty scaler inputs is utilized for data acquisition. Scaler counting is retriggered by the 60 Hz interrupt. Thirty inputs are configured for VFC operation, seven inputs are allowed for I clock and parity signals and the remaining inputs provide a crystal reference oscillator and a time of day feature. An input is provided for remotely resetting the QPM.

The monitor includes a control card to interface with various protection subsystems. This card provides address polling of the "keep alive" HFU's and pulse train enabling of other critical subsystems. Control card facilities include 16 bits of buffered output, 8 bits of pulse train sensing and 24 bits of TTL level sensing. A phase lock loop generates the 60 Hz interrupt from a filtered line voltage zero crossing detector.

## Present Status

Earlier generations of the QPM prototype were implemented with a Z80 based single card computer system. With the evolution to a MC68000 based QPM the Z80 card remains a valuable development tool. Presently the Z80 system operates in a multiprocessor configuration with the MC68000. In this configuration the Z80 provides the analytic and I/O facilities of the host computer. Hardware facilities provided with the Z80 include a floppy disk, console, line printer, and graphics display. These facilities may be used by applications programs written in one of several available languages to store, retrieve, analyze, and display QPM status and data. We are currently testing the foreground protection task in the MC68000 with a debug monitor running in the background. During the early partial ring testing of the Energy Saver systems, the Z80 processor and development facilities will be removed and the MC68000 will provide the system communications as well as the protection function.


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