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THE CONTROL SYSTEMS FOR THE CERN SUPER PROTON SYNCHROTRON RING POWER SUPPLIES

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1. Summary

This paper describes the dedicated control system for the 16 voltage-controlled Main Ring pulsed supplies, allowing the reproduction of the desired B and Q fields to better than $\pm 2 \times 10^{-4}$ at injection. It outlines both the hardware (smoothed function generators) and software side. Current measurements via DVMs or the B train off the reference magnets are used as inputs to the correction algorithm which is based on successive approximation. The algorithm enables the machine operators to trim selectively both the closed orbit and/or the betatron wave number of the machine within 1 to a few cycles. The control system related computer memory requirements are given.

2. Introduction

The CERN SPS is a separated function machine. One set each of bending (BM), focusing (QF) and defocusing (QD) magnets are controlled independently. The QF and QD magnets are each driven by one supply of ±4000 V and 2200 A. The BM supplies are connected in series, each followed by about $^1/_{12}$ of the magnet load. Each MB supply delivers ±2000 V and 7500 A peak, 3200 A RMS. The single supply systems QF and QD are treated exactly like the multi-supply BM system. A single NORD-100 64K computer controls the three systems.

3. The Function Generator (FG)

Reference is made to Fig. 1. The FG is supplied every 10 msec with the digital form of the negative voltage change desired ($-\dot{E}$) during the next 10 msec. The high resolution DAC ≠ 1 is preceded by a digital subtractor, thus inverting the sign. E1 will then have the form of successive steps. By choosing R1·C1 very small and at the expense of very non-linear ramps one could arrive at a stable output voltage at the end of each 10 msec interval. This is avoided by adding DAC ≠ 2 which feeds additional current into the integrator stage, thus improving the linearity of the ramp. The transfer characteristics on step inputs will show for DAC ≠ 1 a d.c. gain of $^5/_3$ with the values indicated, for DAC ≠ 2 the same time constant plus a multiplier R1/R2. Given the fact that a non-attenuated increment is taken at 14 bits full scale, E2 is then equal to -4 times the change at E1. The output must also have increased by $^5/_3$ of the change at E1 after 10 msec if the circuitry performs properly. All this delivers an equation R2 = f(R1). The bigger R1 is, the more linear the ramp. This will however amplify any offset voltages from the less precise DAC ≠ 2. We settled for R1 = 3.48 kΩ with R2 ≈ 3.5 kΩ. Full output is reached within 24 msec.

4. The Correction Algorithm

The pulse shape is defined by its absolute value every 60 ms. A first set of corrections will compensate for slope errors found between two successive values. This relative correction on its own will produce the proper pulse shape. However, it can be offset by any given amount. A second set of corrections is needed to take into account the absolute error every 60 msec. The relative corrections are made from cycle to cycle, i.e. the corrections calculated on the basis of the measurements made during cycle N are applied to cycle N + 1. The absolute corrections on the other hand are carried out within the interval T + 60 and T + 120 ms.

Let us consider Fig. 2a. We assume that the demanded field should be constant, hence all $\Delta B/\Delta t = 0$. The error between T_{N-1} and T_N can be calculated into a voltage correction V_c. This voltage shape is not possible with the integrator type reference. One solution would be the indicated V_c'. It is obvious that the adjusted voltage resulting from a series of (equal) corrections would introduce a considerable amount of ripple, and to avoid this the wave-shape ABCDEFG was adopted.

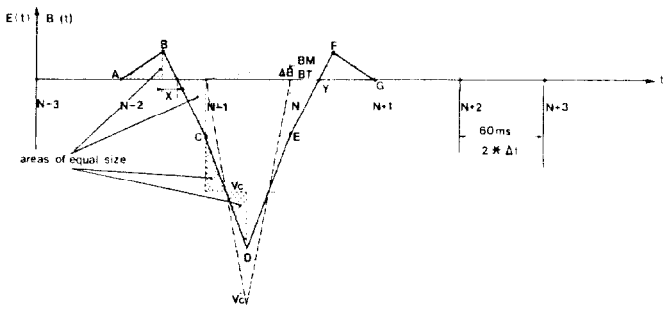

Fig. 2a

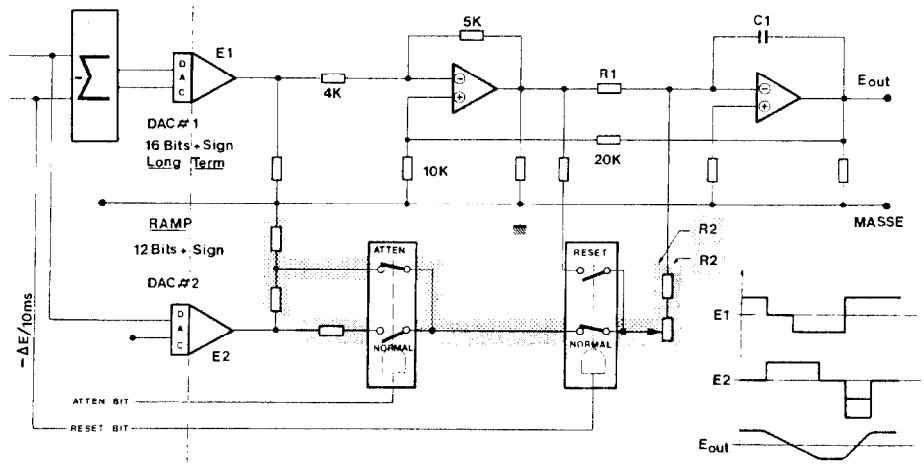

Fig. 1

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The following conditions were imposed:

a) Points C, E are to be at $V_c/2$.

b) $\int_{N-2}^{N-1} V(t)dt = 0$; $\int_{N}^{N+1} V(t)dt = 0$.

Either one of (b) delivers two equations:

1) $(\Delta t + x) \times V(B) + (\Delta t - x) \times V_c/2 = 0$

2) $V(B)/x + V_c/\left(2 \times (\Delta t - x)\right) = 0.$

Solved for V(B): $V(B) = -V_c/4$.

Further, it is obvious that the voltage changes C-D and D-E must be $+V_c$, $-V_c$ respectively if the areas (N-1)-V_c-(N) and (N-1)-C-D-E-(N) are to be equal. Fig. 2b shows the resultant voltage output to the integrator.

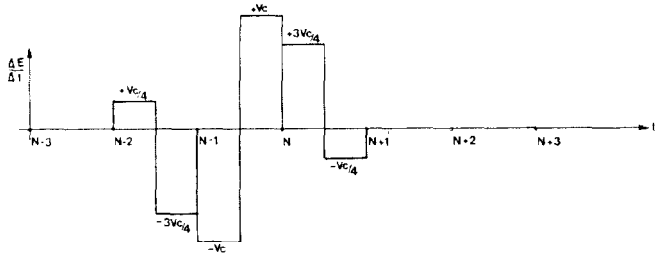

Fig. 2b

Note that the sum of corrective values which are output is equal to 0. Resistive components of the load are neglected. Three consecutive measurement intervals are affected. Thus only at T_{N+1} can the correction terms be fully calculated for the interval T_{N-1} to T_N. The general formulae then look as follows:

$$\Delta E1 = K \times \left(-\tfrac{3}{4} \times \Delta\hat{B}(N-1) + \Delta\hat{B}(N) - \tfrac{1}{4} \times \Delta\hat{B}(N+1)\right)$$

Second 30 msec interval:

$$\Delta E2 = K \times \left(\tfrac{1}{4} \times \hat{B}(N-1) - \Delta\hat{B}(N) + \tfrac{3}{4} \times \Delta\hat{B}(N+1)\right)$$

where $K = \left[V/T\right]$ or $\left[V/T/m\right]$.

The correction values ΔE1, ΔE2 are added to their respective E(t) entries and will take effect during the next cycle (and thereafter).

Fig. 3 shows the relatively smooth correction voltage for the error depicted.

With a different parameter K the absolute correction is carried out along the same lines. Due to the algorithm, the corrections will be applied to the interval (N + 2) - (N + 3) and not to the full force. This is a compromise solution as one does not know whether a "found" ΔB will persist. We opted for a 50% correction. Experience shows that, given an initialization error of up to 10%, the maximum error will be less than 0.03% of demanded value within 10-12 pulses with an I_{MAX}/I_{MIN} range of > 40.

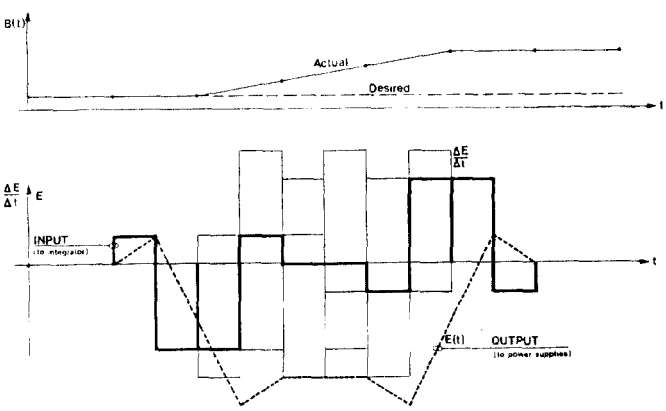

Fig. 3

5. The Data Layout

Most of the data must be readily accessible for read, write or both. Thus it cannot be put on external storage devices like floppies or similar. The longest pulse catered for at the SPS takes 19.2 sec. The following tables are used, 1 per each of the three systems:

- a table defining B(t), (Q(t)) every 60 msec
- a table containing the voltage changes for each 30 msec interval
- optional; a table containing the measured values each 60 msec (for readouts!)
- a general data area for variables like R, I, L, dE/dt(max), limits, table and other pointers, system status, error entries, conversion factors and others.

All this takes up about 10700 locations for the three systems.

6. The Main Driver

6.1 Driving the reference(s)

Each reference gets its specific voltage increment every 10 msec. It acknowledges the receipt of the data via an individual parity line. As the occurrences of data transmission errors have been rather infrequent, the output driver simply records the incidence should a second data transmission also fail. Checks against impossible values or against preset limits, such as maximum and minimum voltages in the supplies, are carried out before any value is sent off.

For the MB supplies the voltage increments are passed through a so-called "splitter" which serves mainly to limit the reactive power taken up by the supplies. During injection and in the initial phases of acceleration of the beam, all supplies must run in parallel at (nearly) equal voltage. Here the splitter will distribute the voltage increments evenly on all stations. Starting at an externally-set level the supplies are split into three groups for the purpose of driving each group as close to the extreme limits as possible. Thus, during acceleration the splitter will first feed group 1 exclusively up to its limit, then proceed with group 2 and finally attribute to group 3 whatever voltage is required. During deceleration and recovery prior to the next injection, the opposite process will take place and finally all units driven in parallel again.

To provide some flexibility, one has divided the whole cycle into ten distinct sequences. Each sequence is defined with a 16-bit word, the lower byte containing the number of 60 ms intervals in this particular sequence (thus limit = 15.3 sec), the upper byte instructions in bit set/reset form to be carried out. Examples are: storage on/off, error calculus on/off, reset period, cycle error update, short absolute correction. These sequence identifiers not only serve the output driver but also the correction program. Fig. 4 shows a simplified layout of the main driver.

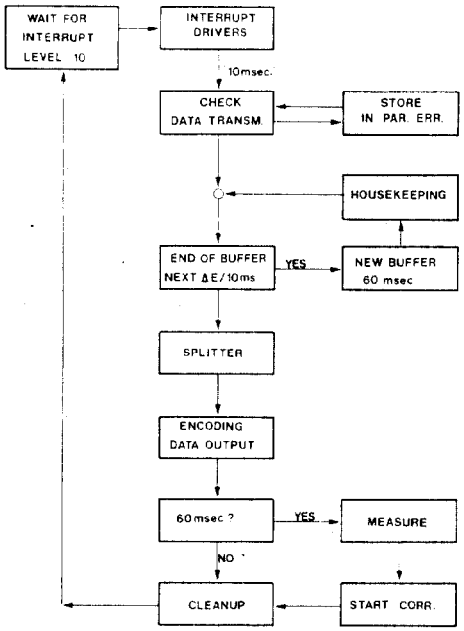

Fig. 4

6.2 Correcting the output

The main driver will read the B-train counter every 60 msec and check whether the sequence is controlled via a DVM or the B-train. The correction program runs one level below the driver(s) and the DE table entries will be updated via the algorithm explained earlier. The whole process has to be finished at least 10 msec before the start of the next 60 msec interval as, as explained earlier, the absolute corrections will then already take hold.

Figures 5 and 6 show the correction set-up both from the hardware and the software side.

6.3 The storage mode

In any given flat-top sequence one can switch into the storage mode which allows the future p-$\bar{p}$ colliding beam experiments. From that moment onwards the corrections will be based on a DVM/current measurement in order to exclude the drifts of the integrator-based B-train electronics. Figure 5 shows this particular

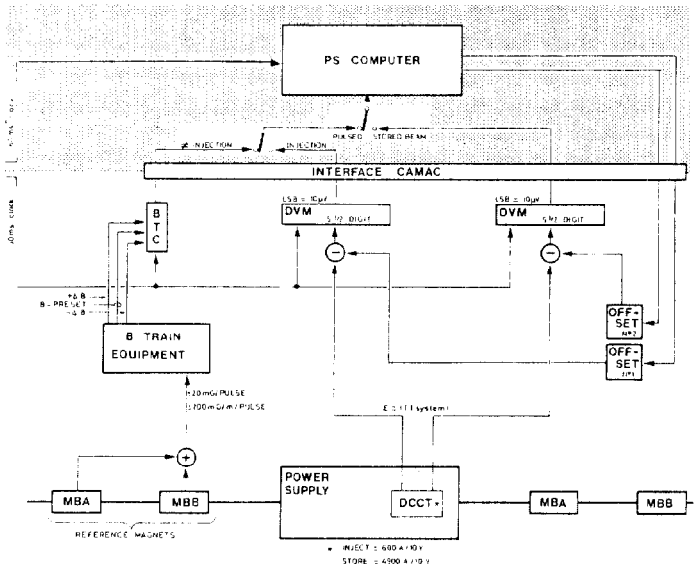

Fig. 5

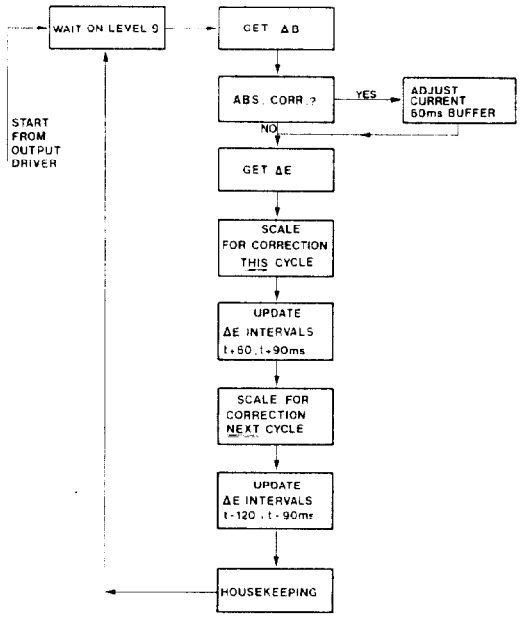

Fig. 6

set-up. As the B-train determined current level is normally what the beam wants, a simple calculation is executed at the start of a storage mode:

$$B(\text{B-train}) \equiv K \times [E(\text{DVM}) + \text{OFFSET}]$$

The factor K is then used throughout the storage phase to convert current into B for the correction algorithm.

After an externally-set number of SPS cycles has elapsed the software will switch back into the pulsing mode and finish off the remainder of the pulse which was started earlier. This method of inserting "coast" periods of a length $\equiv N \times$ SPS cycle length allows it to remain absolutely synchronous with the other CERN machines. For example, it allows the insertion of one coast cycle at the injection level every cycle. This new "normal" cycle then has a double length of say 2 × 12 sec with an injection area of X + 12 sec allowing multibatch injection tests. The software provides the possibility of specifying these coast periods at up to three different levels during a given cycle.

6.4 Core requirements, execution times

Again, the above-described programs must be resident. The main driver, the correction and splitter programs and the DVM drivers plus various routines, take up about 3000 locations. Executing the above-listed tasks takes about 3.5 msec/10 msec interval at level N. At level N-1 (corrections) about 10 msec/60 msec interval is required. The average CPU load is of the order of 50% per 60 msec interval.

7. The operators' involvement

If, with the help of some high-level programming, the operator wishes to adjust the status of the machine (say the Q of the beam) he simply overwrites the existing B(t) table entries. This adjustment will manifest itself as a one-time error to the correction program. The program will act on it and, after 1 to a few cycles, the equilibrium will be restored. Drifts in an element will be to almost 100% anticipated by the program and thus rendered invisible to the over-all system. Likewise the resistive component in the load is taken care of by the algorithm.

The use of rather large amounts of memory allows the rapid display of the status and behaviour of each of the three systems, and thus helps considerably in error detection, analysis and correction.