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60 MHZ 6 BIT DIGITAL TO ANALOG CONVERTERS FOR THE SUPER BEAM DAMPER OF THE FERMILAB MAIN ACCELERATOR

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Introduction

Two of these high speed Digital to Analog converters were designed and built for use in the super beam damper of the Fermilab main accelerator.[1] They are replacements for an earlier less stable version.

With complementary digital inputs, the converters provide complementary outputs of a digitally delayed beam position analog signal. Both D/A's are capable of converting a six bit digital word to ±2.5 volts into a 50 Ω load with DC response, typical rise and fall times of 5 nanoseconds, and long term stability. Conversion speeds of 60 MHz are easily obtained.

Hardware

Figure 1 is the block diagram of the circuitry. The heart of the converter is a ring of six high speed comparators[2] with current source outputs. This circular arrangement allows for an equal time delay of the summed currents. Each of the currents is weighted appropriately by the adjustment of a trim potentiometer.

The currents are precisely regulated by a stable voltage reference. Figure 2 is a photo of the comparator ring and voltage regulating circuitry.

*Operated by Universities Research Association, Inc. under contract with the U.S. Department of Energy.

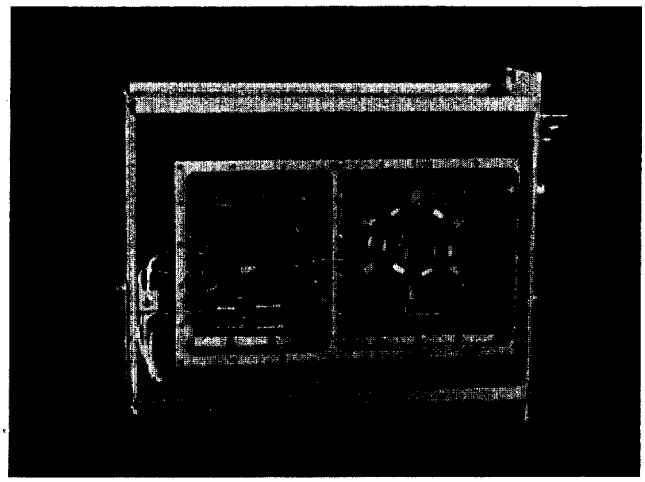

Figure 2. D/A comparator ring and regulation circuitry.

The output stage consists of a high speed operational amplifier[3] with a DC gain of approximately 2.5 and feedback compensation for the reduction of transient overshoot. The six output currents are summed into a load resistor. The resulting voltage is then amplified by the op amp and is the reconstructed analog signal. The output must be terminated by 50 Ω load impedance.

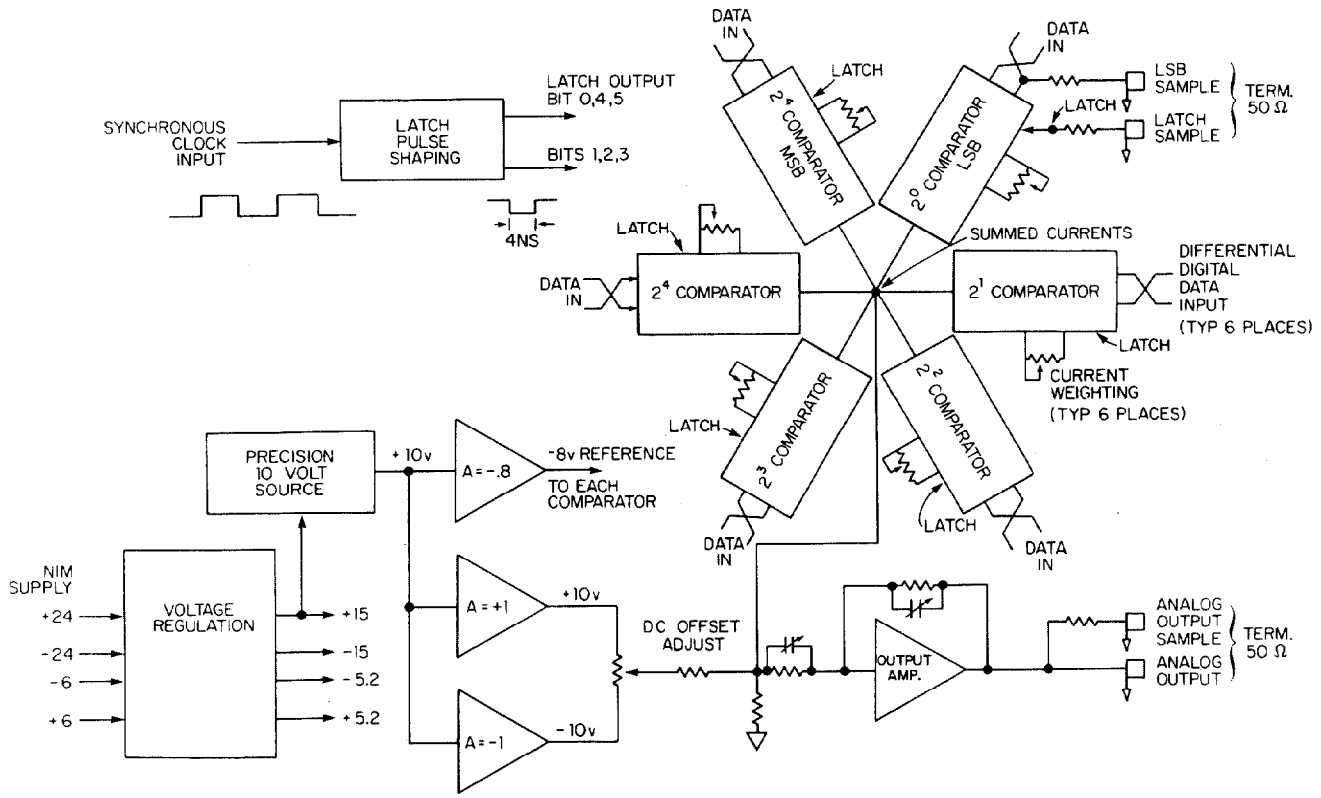

Figure 1. 6 Bit 60 MHz D/A Block Diagram

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The hardware is built in a segmented milled block of aluminum and housed in a 2 wide NiM module. The aluminum provides RF shielding, heat sinking, and a sealed enclosure.

Time Considerations

The D/A's receive a six bit digital word and a synchronous clock from a digital fanout network in the super damper system. All signals are ECL 10K logic levels. The clock when received is approximately 50% duty cycle. A pulse shaping network converts the clock to a negative latch pulse 4 nanoseconds in width. The six bit data is received differentially and applied directly to the comparator inputs. The positive edge of the latch pulse occurs 5 nanoseconds after data transitions have settled. Adjustment of the latch timing is accomplished with delay lines located in an exter·ıl digital fan out network. Timing monitor points ·e provided on the front of the NiM module for thi· ·urpose (Figure 3). The output current is maintained until the next latch pulse.

Figure 3. Front View of D/A.

Performance

A digital word generator built into the fanout logic allows for testing of the D/A's. A reconstructed ramp from the digital word generator is depicted in Figure 4. The glitch at the base of the ramp is caused by the need of an extra clock pulse to load the counter in the word generator.

As stated earlier, two of the converters are used to provide complementary outputs, hence identical through put delays are desirable. Measured delay from latch pulse to analog output is 20 nanoseconds. Figure 5 shows the complementary outputs for a maxiumum rate of change from $+2.5$ volts to -2.5 volts. Transition times are on the order of five nanoseconds with low overshoot.

Temperature stability is achieved by the stable reference voltage and adequate heat sinking of the comparators and output amplifier.

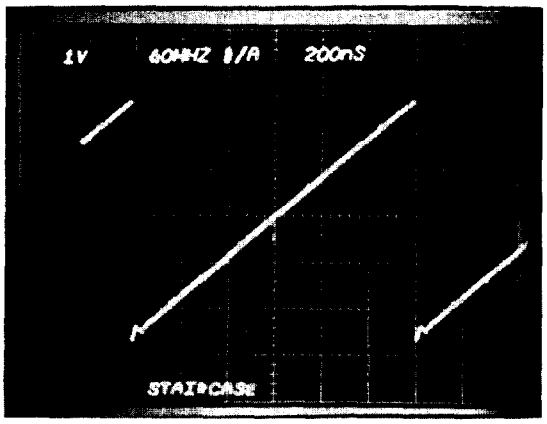

Figure 4. Output Ramp Waveform

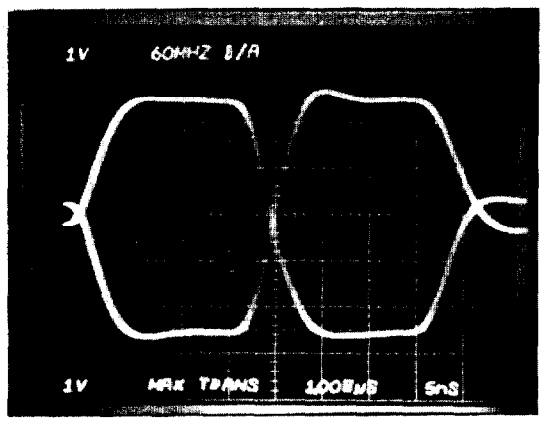

Figure 5. Output Under Maximum Transition Conditions.

Conclusions

In its application at Fermilab, the units operate at a conversion rate of 53 MHz. The D/A's have been in continuous operation for one year without need of readjustment.

Acknowledgments

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