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A CAMAC SERIAL CRATE CONTROLLER FOR THE TEVATRON ACCELERATOR

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Summary

A CAMAC serial crate controller has been developed for the Tevatron Accelerator Control System. The controller accommodates two serial ports of access, block transfer read facility, and aggregate command capability. Communications to the controller are bit serial at a 10 megabit rate and employ a specially developed protocol. The programmed serial ports allow better than 50K dataway operations per second. The Block Transfer read facility operates in the UQC mode and can perform at the rate of 250K dataway operations per second. Operations at both ports and the Block Transfer function may be fully interleaved. The design provides for programmed arbitration of the two serial ports allowing either port to reserve the crate or a target slot for an uninterrupted sequence of dataway operations.

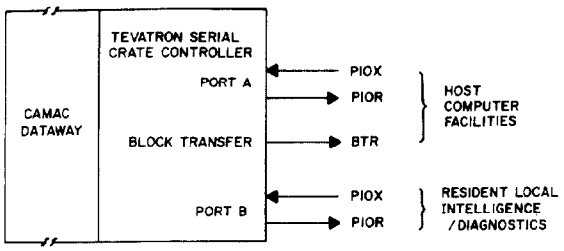

Fig. 1. System connections to the TSCC.

System Considerations

Controls for the Tevatron accelerator are being implemented with CAMAC crates as the primary interface between host computer facilities and Tevatron subsystems.[1] It is expected that the control system will eventually be comprised of more than sixty crates distributed around the accelerator's 6.28km circumference. CAMAC, an established IEEE standard supported by a wide variety of commercial and in-house designs, is often implemented in accelerator environments. Though not without failings, the CAMAC convention is a relatively powerful and efficient bus structure for process I/O applications.

From the very early stages of specification, it was apparent that the Tevatron control system should accommodate a large number of microcomputer subsystems and local interactive facilities. The data base for the system is easily one to two orders of magnitude larger than that of the existing Main Ring. Interaction between subsystems at the service building level was anticipated as either module-to-module or crate-to-crate data transfers. Commercially available controllers and standard protocols did not satisfy these requirements. Additionally, the CAMAC environment was not viewed as especially appropriate for general purpose microcomputer systems.

Controller Characteristics

The TSCC is a two-ported controller designed for a 10 megabit/sec bit serial synchronous control network. Data transmissions to and from the controller are 50 ohm compatible, low-power, self-clocking, and employ the Manchester Bi-Phase code. Accelerator wide communications with control system crates are accommodated by a serial data repeater system which is compatible with this code.[2] Port A is the host computer port and has separate input and output lines (PIOX and PIOR). Port B is also a serial port and is generally symmetric to Port A. Port B is intended to accommodate local microcomputer and diagnostic facilities. The TSCC also provides a block transfer return (BTR) path to the host. This BTR function, controlled only by Port A, shares operation of the CAMAC dataway with Ports A and B.

The TSCC as implemented maintains the dataway conventions of IEEE 583 while rejecting the serial highway standard, IEEE 595, as inadequate for implementation of the Tevatron control system. Adoption of the 10 megabit/sec serial rate was predicated by the large distributed nature of the system, the increased data base, and the desire to support fast interactive facilities at the Main Control Room.

The unique aspect of the TSCC is the feature of programmable arbitration of the CAMAC dataway by either of the two ports. Communications with a target slot or the entire crate may be exclusively allocated to either Port A or B for multiple dataway cycles. This feature accommodates uninterrupted communication with microcomputer based subsystems typically requiring multiple data transfers. In addition, the TSCC arbitration capability prevents Port A or Port B from communicating with a crate module that is actively returning block transfer data.

CNAF commands from a host facility driver are transmitted to all system crates simultaneously on the Port A PIOX line. Only the addressed crate responds over the PIOR line.

Serial Data Protocol

All data transmissions to or from the TSCC contain either 16 or 24 bits of data. Each transmission has a two bit header and tailer forming a complete 20 or 28 bit frame. Normally sequential frame transmissions are separated by 300 nsec. Even parity of the frame is preserved by a parity bit in the frame tailer.

Port A PIOX Operations

The first frame transmitted to Port A over the PIOX line includes an eight bit crate address and arbitration requests as follows:

SCRA: Set Crate Reserve for Port A
SNRA: Set Slot Reserve for Port A
RCRB: Reset the Crate Reserve of Port B
RNRB: Reset the Slot Reserve of Port B

The received crate address is compared against two internally selected addresses. The first address is unique in the network and the second is an aggregate address common to more than one crate.

The NAF information is transmitted in the next frame. N(0) through N(23) specify a dataway cycle with F(0) through F(7) indicating read operations and F(16) through F(23) indicating write operations. N(24)

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specifies an operation targeted to the crate controller as follows:

F(0)·A(0)	- Requests a response transmission of the state of all LAM's in the crate.
F(4)·A(0)	- Toggles an internal ON LINE/OFF LINE flip-flop.
F(8)·A(0)	- Sets the Inhibit line.
F(12)·A(0)	- Resets the Inhibit line.
F(16)·A(15)	- Sets the BTR function.
F(20)·A(15)	- Terminates the BTR function.
F(24)·A(15)	- Causes a C·S2 cycle.
F(28)·A(15)	- Causes a Z·S2 cycle.

If present, the third frame is normally 24 bits of write data. If the BTR function is being set, the third and fourth frames indicate target NAF, word count, and the maximum allowable number of sequential no Q's. These latter two parameters have ranges from 0 to 65,535 and 255 respectively.

Port B PIOX Operations

The first frame transmitted to Port B includes crate address and arbitration requests as follows:

SCRB: Set Crate Reserve for Port B.
SNRB: Set Slot Reserve for Port B.

The second and third frame, if appropriate, contain NAF information and write data.

Crate addresses received by Port B are not compared to the aggregate address. Port B has no capability of removing Port A crate or slot reserves. The only N(24) controller operation available to Port B is requesting the return of LAM status.

Controller and Dataway Cycling

Four service request levels prioritize the execution of dataway and controller operations. The first level is raised in response to the application of dc power and causes a Z·S2 initialization cycle to be executed. The second level is raised in response to a properly addressed Port A PIOX transmission. The third level is repeatedly raised by the internal BTR function when active. The final level is raised in response to a properly addressed Port B PIOX transmission. Service request levels raised by either Port A or B result in responses on their respective PIOR lines, the only exception being Port A aggregate commands. Only BTR dataway cycles that receive a Q generate responses on the BTR return line. Requested operations from Port A or B may be denied by an arbitration conflict or a detected protocol error. Port A, Port B, and BTR operations may be fully interleaved. The maximum delay encountered by any of these operations is 1.5 microseconds.

Port A and Port B Responses

Responses from either Port A or B consist of at least two 28 bit frames containing three bytes of controller status and the echoed CNAF command. If present, the third 28 bit frame contains read data, echoed write data, or individual slot LAM status. Status information includes Q, X, I, the state of Port A and B reserves, the state of the BTR function, and indication ofany asserted LAM. Flags indicating that a Port B crate or slot reserve was terminated by Port A are also provided.

BTR Responses

All responses on the BTR line are 28 bit frames containing either status or block transfer data. The status frame is transmitted at the beginning and end of the variable length data block. Included in this status are the crate and target slot addresses, and flags which indicate the cause of BTR termination. BTR normally terminates on decrement of word count to zero, but may also be terminated by excessive no Q's or by a timeout.

Current Status

The TSCC is being implemented as a four board module set resident in the CAMAC crate. Prototypes have been successfully operated in the A-sector of the Main Ring since early fall of 1980. Current schedules call for installation of controllers in half of the Tevatron service buildings by fall of 1981. A TSCC Link Driver has also been built to permit interface of central host and local computer facilities. The Link Driver performs necessary parallel/serial conversions and renders the particulars of the 10 megabit/sec serial protocols transparent to the user.

As measured from the Link Driver, without cable delays, more than 50,000 programmed I/O data transfers per second (150K bytes/sec) are possible. Block transfer rates can approach 250,000 frames per second (750K bytes/sec), top speed being typically limited by the block data source.

Acknowledgements

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References

1. D.Bogert, et al., "The Tevatron Control System," paper E-24 of this Conference.

2. R.Ducar, "Tevatron Serial Data Repeater System," paper E-60 of this Conference.