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THE TEVATRON CONTROL SYSTEM

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Abstract

The Tevatron Control System is a large distributed facility controlling the 6.28km Tevatron Accelerator from more than thirty distinct control locations. The system employs CAMAC hardware as the primary control interface. Self-cycling microprocessor based systems that utilize more suitable computer bus architectures are readily accommodated. The scale and nature of the Tevatron warrants special consideration as to system throughput and snapshot data handling. Computer based facilities can be provided at the service building level to assist host computer functions and to permit local diagnostics.

Introduction

The control system for the Fermilab Tevatron accelerator is designed to operate in an integrated fashion with the control system for the existing Fermilab accelerator complex. The existing accelerator is a three stage operation consisting of a 200 MeV RF Linac, an 8 GeV/c RF synchrotron Booster, and a 500 GeV/c RF synchrotron Main Ring. The bending dipoles of the Main Ring are conventional copper and iron water cooled magnets having a maximum bend field of 22 Kg. This conventional accelerator has operated for eight years. The motivation for the Tevatron, also known as the Energy Doubler/Saver, is at least two-fold. First, the addition of a second ring of superconducting magnets in the Main Ring tunnel can result in power savings if 150 GeV/c protons are transferred from the Main Ring and accelerated to 500 GeV/c in the superconducting accelerator. Secondly, if the entire 6.28 km circumference is filled with superconducting dipoles of 45 Kg full field strength, the peak energy can be doubled to approximately 1000 GeV. A planned additional mode of operation calls for use of the superconducting accelerator as a long term storage ring for colliding $p/\bar{p}$ experiments. Such operation would require tens of hours of continuous operation at full field, a mode that would be prohibitively expensive in an accelerator of conventional magnets. Thus, it is necessary to regard the superconducting accelerator as an integrated addition to the existing complex properly sharing a common control computer network and operations center.

Control System

Part of the instrumentation development for the Tevatron project includes the simultaneous replacement of the present "host" or "central" computer system of the Fermilab accelerator complex. The existing accelerator has been managed by a family of five essentially decoupled Xerox Data Systems 530 central processors. The control consoles for each system (Linac, Booster, Main Ring, development areas, etc.) are coupled to individual XDS-530's, with the result that most types of cross-system control interactions are impossible. A new and more centralized host computer system including the requirements of the Tevatron was specified in early 1980 and bids were solicited. The successful response was from Digital Equipment Corporation with a proposed network of twelve PDP 11/34's and two Vax 780's.

The Tevatron, however, has certain timing and control requirements that prevent the concentration of all control decisions in a central computer. These requirements are, in part, the result of the greatly increased difficulty of operating a very extended set of superconducting magnets. These magnets have several very "fragile" properties. Most significant are the consequences resulting if some localized segment of the super conductor goes normal. The resulting heating can rapidly lead to melting and destruction of the superconductor. This process is so rapid that protection cannot be guaranteed by control from a distant host computer. Other distributed control functions are also needed where timing requirements dictate. The parallel development of hundreds of correction functions in real time and the operation of thirty satellite refrigerators are but two examples. As a result, the Tevatron control system consists of specific central host functions coupled to distributed intelligences located in the thirty local service buildings.

The Tevatron control system is composed of a number of primary elements. The Central Host System includes operator's consoles each driven by a PDP-11/34. Each PDP-11/34 is connected to one of the two VAX 780's, which acts as a network communications manager, as well as (in conjunction with the other VAX-780) a central calculation and data storage facility. Also network connected to the VAX-780 is another PDP-11/34 which acts as a "front-end" for the Tevatron System Link.

The Tevatron Link is a high speed, low noise data communications system. Information is carried on the link using a self-clocking Manchester Bi-Phase code operating at a 10 megabit/sec rate. For long range transmission a repeater system located at each of the service buildings demodulates and remodulates the Bi-Phase code to a 50 megahertz carrier frequency. Signals are transmitted between service buildings, a distance of some 260 meters, over a buried nineteen conductor Andrew Heliax cable. Control functions allocated to this cable include separate transmit and receive programmed I/O functions (PIOX and PIOR) for communication with the service building CAMAC crates, and a high density block transfer return (BTR) facility. Other signals include an encoded real time clock operating at 10 megahertz, a dI/dt clock from which one may integrate the Tevatron dipole current, a beam abort, a power supply abort, and possibly several others. The serial control links for the existing Main Ring may be added to this cable at some future time.

The Tevatron front-end PDP-11/34 interfaces to the CAMAC serial link via modular Link Controller and Driver devices. First versions of these devices are in operation while final versions are in development.

The Service Building CAMAC Crates are the basic building blocks of the Tevatron Control System. Communications with these crates consist of standard CNAF and data transmissions over the Tevatron link. The crate controller is an in-house Fermilab design that

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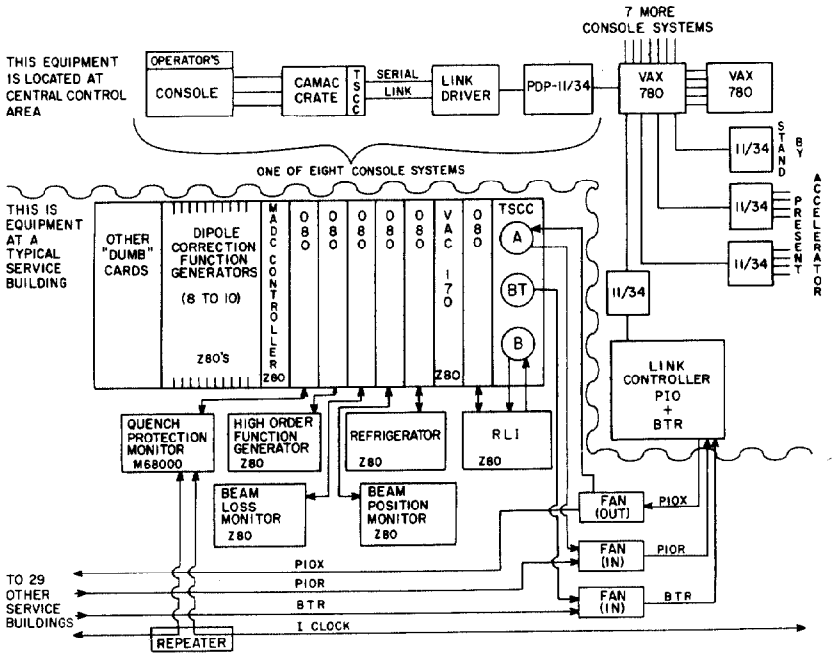

Figure 1. Logical Representation of Tevatron Control System

conforms to the IEEE 583 dataway conventions. The controller does not, however, conform to the IEEE 595 serial standard. The Tevatron Serial Crate Controller (TSCC) supports two separate, symmetric, 10 megabit/sec serial ports, Port A and Port B. The TSCC supports a Block Transfer Read function, and also aggregate commands from Port A. The TSCC supports programmed arbitration. Both Port A and Port B have the capability to reserve the entire crate or a target slot for multi-cycle operations. Additionally, the block transfer function locks out Port A or B operations to the BTR target slot.

CAMAC is not ideal for interboard communications of data under the control of an on-board microprocessor, since CAMAC was designed to be more typically an extension of an I/O bus of a central computer. Slot to slot communication of data can be readily accommodated only by the inclusion of an additional bus or via an intelligence located in the crate controller. The use of an "intelligent" crate controller is possible, but the data transfer rate typically is slow. Whether to package a subsystem externally or in the CAMAC crate was dictated by its size and complexity. The choice of most designers of external subsystems was to package the subsystem in an INTEL Mulitibus crate.

The logical structure of the subsystems supported by a CAMAC crate in a service building is illustrated in Figure 1. At least nine different types of subsystems are shown, each including a microprocessor. These include: vacuum, refrigeration, quench protection monitor, beam position monitor, beam loss monitor, dipole correction function generators, higher order function generators, resident local intelligence, and multiplexed ADC controller. Some of these subsystems, such as vacuum, are shown resident in CAMAC. Others, such as refrigeration, are external to CAMAC and are interfaced through a CAMAC 080 module.

The Microcomputer Standards attempt uniformly to define the software and, to a large extent, hardware architecture of subsystems. An early decision was to standardize the microprocessor. The original choice was the ZILOG Z80, a choice dictated as much by software development capabilities as anything else. All systems except the Quench Protection Monitor System now use the eight bit Z80. The timing and complexity of the QPM dictated a switch to the more powerful sixteen bit Motorola 68000. With the exception of the dipole correction function generator, which is functionally decoupled from the host intelligence, all of the other eight types of microprocessor subsystems have rather direct host to intelligence coupling. These couplings envision the exchange of relatively long data streams of arbitrary configuration. A software protocol to define these exchanges has been specified and is known as GHASP (General Host and Subsystem Protocol). The specification of GHASP, which occurred after some subsystem design and production had begun, did not resolve the difficulty of the need for eight different software driver/receivers on the subsystem side of communications. That this would be a major complication was not clearly perceived in the earliest stages of Tevatron Controls development. It is now clear that a reduction from eight subsystem driver/receivers to three is possible, and desirable. This has required the careful definition of three types of systems and the requirement that each of the eight subsystem microcomputers adhere to the basic electronic design standards of one of these three choices. The vacuum subsystem is an example of one of these classes of systems. The vacuum system micro computer is built around the ZILOG family of peripherals. The other classes of subsystems are all external subsystems connected to CAMAC via a CAMAC 080 module. The 080 module has a double stack of FIFO memory, one for outbound and one for inbound data flow.

A general hardware interface to the 080 module using an AMD 9517 DMA has been specified and is in conformance with the GHASP protocol. When packaged in Multibus, this interface will permit communications from subsystems whose microcomputers are either Z80 or

M68000 based. This board is designed to permit a change of microcomputer without any alteration of other hardware. All the Z80 based external system microcomputers have now been defined to have the same basic architecture: Z80 cpu, AMD9519 interrupt controller, AMD9517 DMA, and AMD9513 clock timer. Also AMD9512 arithmetic processors are specified because they match all floating point conventions of the host system. It is thus possible to write only three susbsystem GHASP handlers. These are 1) for Z80 based CAMAC subsystems, 2) for Z80 based external sytems and 3) for 68000 based external systems. The GHASP handlers are standard in all similar systems and act as a basic operating system/communications handler package. The consequence is that system-wide changes may be implemented at a later date with more facility.

The Nine Intelligent Subsystems are illustrated schematically in Figure 1.

1) The Vacuum System has the job of scanning the status of vacuum and controlling the state of all the pumps, gauges, valves, etc. of the insulating and bore-tube vacuums within the domain of each service building. The control microcomputer is packaged in a two slot wide CAMAC module with attendant device interface accomplished in an external crate.

2) The Refrigeration System, which is an external Multibus system, has the job of operating the satellite refrigerator located at each service building. There are 12 closed loops to control, each consisting of a process variable and a control element. Control must continue in the event of loss of communications with the host and resume automatically during recovery from any power outage.

3) The Quench Protection Monitor System, which is another external Multibus system, uses a M68000 for its microprocessor. This system has the job of scanning all magnets for an unexpected change in the voltage drop across the magnet, which would be an indication of a developing quench of the superconductor. In this event, the beam must be aborted and the magnet bypassed with a direct short across the windings. A heater is fired which warms the liquid Helium to 80°K to spread the "normality" throughout the entire winding, thereby removing any local heat concentration.

4) The Beam Position Monitor System has the job of measuring the beam location to ±.1 mm accuracy with Beam intensities ranging from single bunches of about 5×10^7 protons to large bursts of bunches. Intensity measurements are possible with the BPM system, as well as the measurements of $\bar{p}$ pulses rotating in the opposite direction of the standard proton beam. Fast digital averaging of beam position over several turns is calculated by the BPM. Position/intensity versus time information is internally stored for later analysis upon trigger of the beam abort system. Magnet quenches may be induced by the energy deposition resulting from a mis-steering of the beam into the wall and coils of a superconducting magnet. Detailed time development of beam position, as provided by the BPM, is critical to the understanding of orbits and to the prediction of corrective action by the correction elements.

5) The Beam Loss Monitor System is similar to the Beam Position Monitor system in that it saves data in time-ordered lists for analysis of beam intensity losses. Both the beam position and beam loss systems are external, though not packaged in Multibus crates. They do adhere to the minimum microcomputer design standards for GHASP communication via a CAMAC 080 module.

6) The Dipole Correction Function Generators are curve generators designed to construct functions of the form $I_c(i,t) = i*(f(i) + g(t))$ where i is the main dipole current and t the real time elapsed since a "mark" on the real time elapsed clock. These function generators operate on fixed format data tables which are loaded via usual CAMAC CNAF commands. They do not utilize "GHASP." The precision is specified as 2^{-12}.

7) Higher Order Function Generators, are specified to have an output smoothness of 2^{-16}. These develop a real time correction current $I_{HC} = h(t)$. They are external systems mounted in Multibus, designed to handle the more demanding accuracy of the higher multipole correction elements.

8) The Resident Local Intelligence is designed to support several localized functions. It may access any local subsystem via the CAMAC TSCC Port B in accordance with the GHASP protocol. Summarized information from other subsystems may be displayed in engineering units or volts or other "raw" numbers on a local CRT monitor. In addition, the RLI may be used to scan and concentrate alarm information from all of the subsystems, and report changes in alarm conditions to the host.

9) The MADC Controller is a general purpose scanner and logger of analog signals from any other part of the Tevatron not specifically covered in the other intelligent systems. The MADC will also allow plotting of up to four channels simultaneously at a user determined frequency.

The Tevatron Clock is a 10 MHz line sychronized clock carrying up to 256 distinct markers for indication of accelerator events. These markers may be positioned to 100ns accuracy. A special encoder writes these markers onto the clock using the Manchester Bi-Phase standard. The clock is decoded by a hybrid chip under development.

Abort Requests to remove circulating beams and switch the protons onto a dump may be generated by a number of the subsystems, but especially by the BPM and QPM. The abort line is carried to all the service buildings via Transmitter/Receiver repeater modules.

Schedule for Development and Production

The new host computer components have been delivered in the first weeks of 1981. The utilities subsystems (Vacuum, Refrigeration and Quench Protection) have been designed and are being tested in several environments. A full-scale ground level test facility located at B12 has permitted study of controls for the utilities in an evolutionary fashion. The host function was provided by a local PDP-11 at B12. These basic systems, plus the Resident Local Intelligence, will also be tested this Spring in tunnel tests at A2 and A3 service buildings. These tests are also evolutionary since the central host function is being provided by the old XDS-530 system. However, the full capability of the 10 megabit/sec serial link has already been tried and the basic structure of GHASP, the prototype Link Driver and Serial Crate Controllers has already been confirmed as operational.