IEEE Transactions on Nuclear Science, Vol. NS-28, No. 3, June 1981

SNAPSHOT DIGITIZER SYSTEM FOR FERMILAB MAIN ACCELERATOR

Ralph J. Pasquinelli
Fermi National Accelerator Laboratory*
P.O. Box 500
Batavia, Il. 60510

Introduction

The snapshot digitizer system is becoming an important diagnostic tool for the Fermilab main accelerator. This high speed data acquisition system operates at 53 MHz. Inputs to the system are various beam processors whose analog outputs may be digitized and stored in any combination of groupings; i.e. diagnostic mode, starting on any of the 1113 bunches, digitizing 1-1113 sequential bunches, with anywhere from 1-9999 turns around the 4 mile accelerator between digitizations. The system can be gated on at any point of the machine cycle. One of the variations is a Beam Quality mode where each bunch of each of the 13 Booster accelerator batches is tracked and digitized on its first pass around the main accelerator, thereby showing a profile of the injected beam. The combinations of data acquisition grouping are numerous. This paper describes the hardware and timing necessary for the system to operate. Figure 1 is the system block diagram.

60 MHz 6 Bit A/D & Source Multiplexer

At the front end of the data acquisition system are two 60 MHz 6 Bit A/D converters and one analog source multiplexer. The source multiplexer allows remote or local selection of up to six analog inputs for one of the A/D's. It consists of a 6PST coaxial switch and selection logic. At this time, 3 of the six inputs are in use. The system is expendable to the other A/D if additional input capacity is required. The A/D converters presently are specially fabricated hybrids from Hughes Aircraft. They are specified to digitize an input signal with rise and fall times of 2 nanoseconds and a flat top of 8 to 10 nanoseconds at a 60 MHz rate. The input amplitude range and impedance are ± 2.5V and 50 OHMS, respectively. The unit is housed and powered in a 2 wide Nim module as shown in Figure 2. The support circuitry includes voltage regulation and bypassing, timing sample ports, and 10K ECL digital output buffers. The units are constructed in milled out aluminum boxes which afford RF shielding, heat sinking, and a sealed enclosure. Coaxial cables transfer the data and conversion clock to and from the memory.

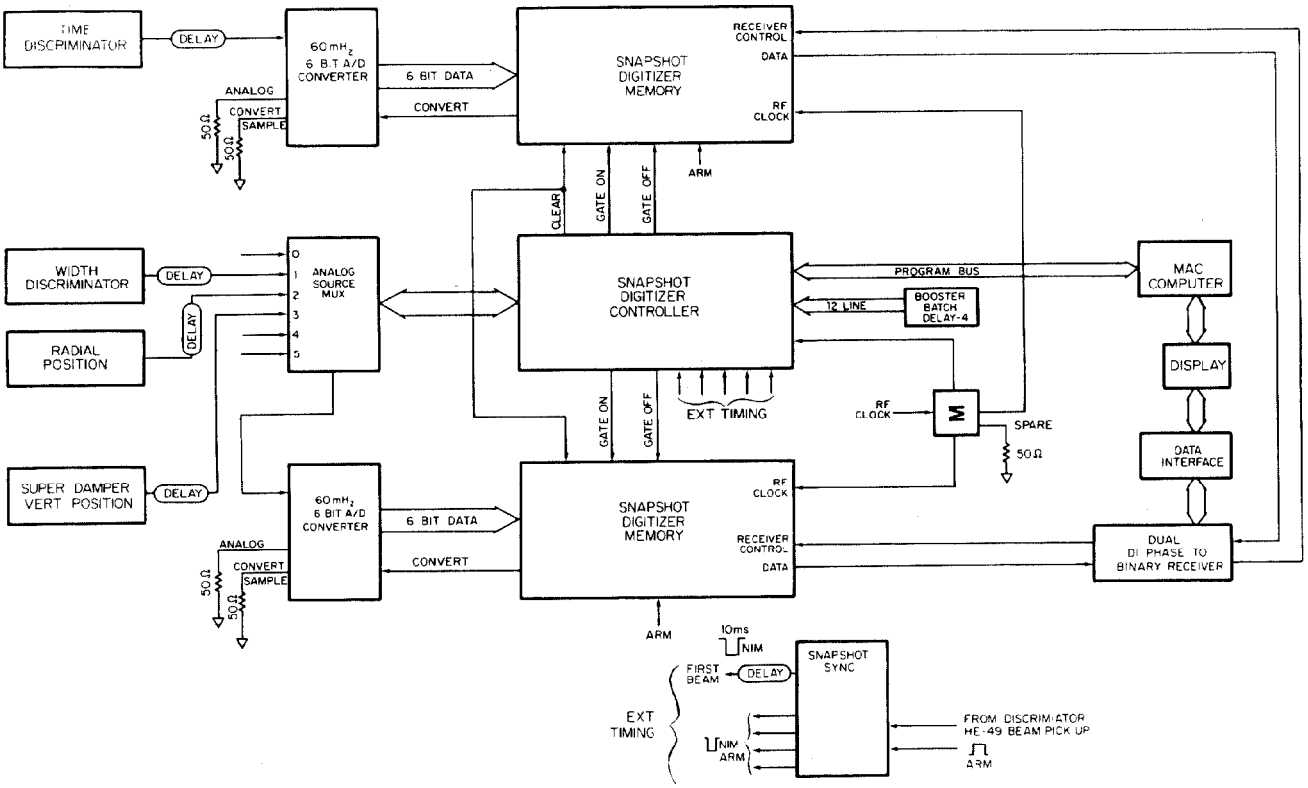

Figure 1. Snapshot Digitizer System Block Diagram

*Operated by Universities Research Association, Inc., under contract with the U.S. Department of Energy.

0018-9499/81/0600-2168$00.75©1981 IEEE

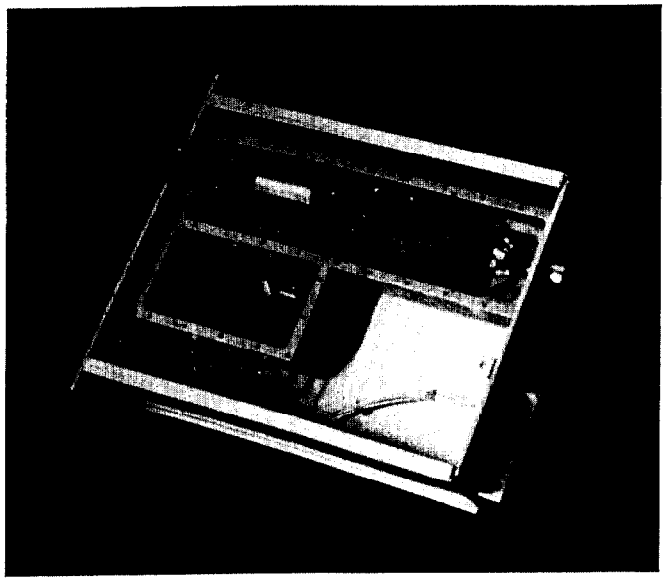

Figure 2. 60 MHz A/D Hardware

Memories

Two identical Biplar ECL memories serve as the fast scratch pad for the system. Each memory is capable of storing 1536 8 Bit digital words at a 60 MHz rate. At present, only 6 of the 8 bits are used due to the limitations of available high speed A/D converters. Because of the fast access times required, the memories had to be divided into left and right halves. One of the halves is addressed every other clock pulse. (See Figure 3) The timing control portion regulates all of the input and output multiplexing, generates the conversion clock for the A/D, and provides external gating inputs. A parallel to serial converter/transmitter relays the data to a remote receiver for loading into a computer.

The hardware is constructed using wirewrap backplane boards. Figure 4 shows one half of the memory and portions of the input and output circuitry.

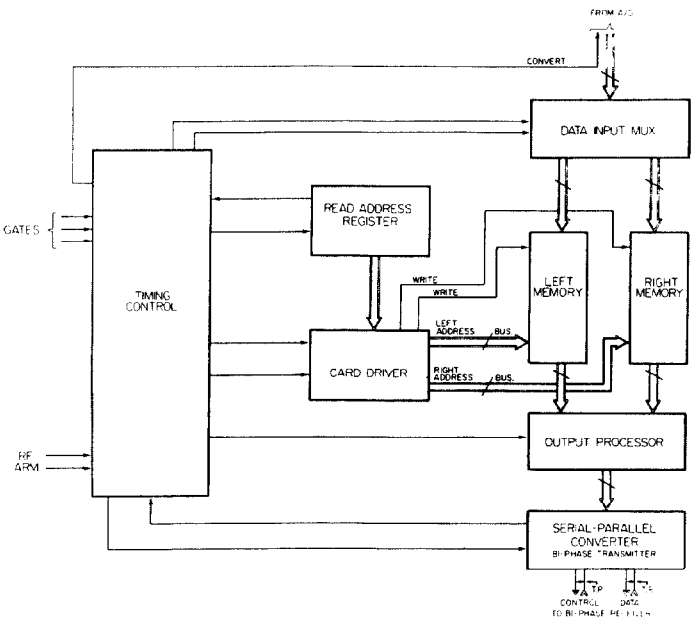

Figure 3. Memory Block Diagram

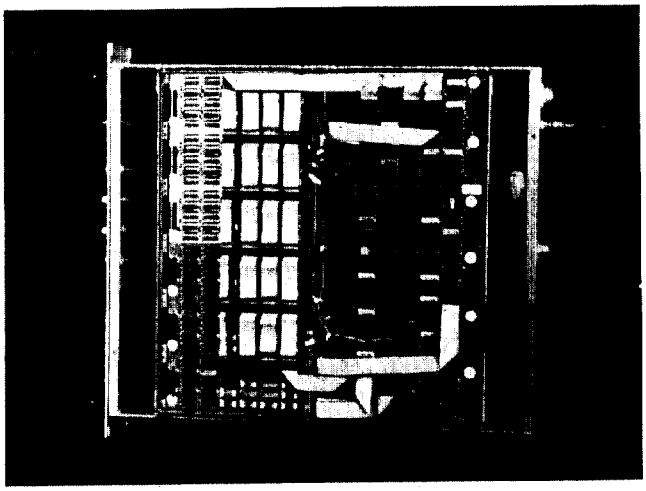

Figure 4. Memory Hardware

Controller

The controller provides precise gating to both memories simultaneously. Five programable high speed counters and associated timing control constitute the heart of the unit as indicated in Figure 5. One of the counters tracks each of the following parameters: 1) J number of turns between digitizing, 2) revolution frequency 53 MHz ÷ 1113 bunches for Fermilab Main Accelerator, 3) start digitizing on Mth bunch, 4) digitize N sequential bunches, and 5) Booster batch delay.

The last counter; i.e., BB Delay, is used only in the Beam Quality mode described earlier. This counter inserts a delay into the Revolution frequency counter to allow for the delayed injection of beam from the Booster Accelerator. The delay is inserted synchronously after each batch is injected. Without this delay, the system would digitize the same Booster batch repeatedly rather than subsequent batches.

The timing circuitry connects all of the counters to produce the desired gates. All of the high speed circuitry is 10K ECL. M, N, J and BB delay counters are remote or locally programable. Sync pulses are available on the front panel for each of the counters.

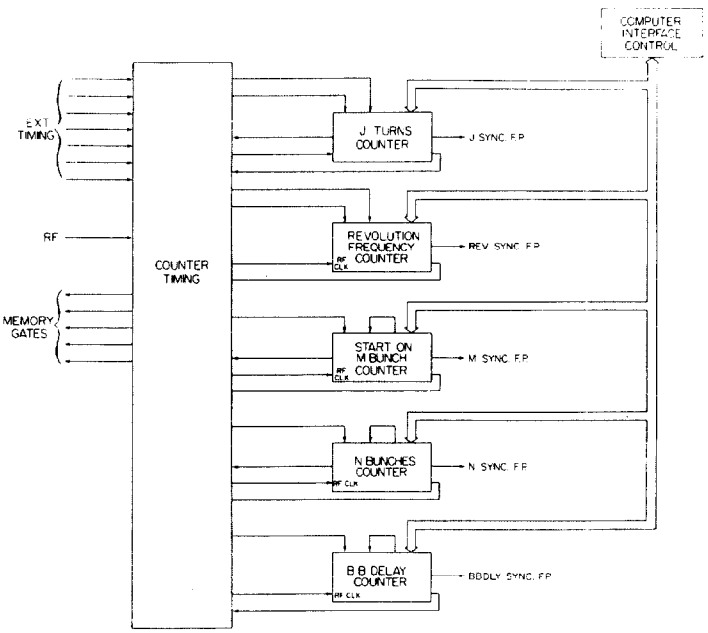

Figure 5. Controller Block Diagram

A snapshot sync circuit provides fan out for all the arm pulses in the system. It also provides a one shot pulse indicating presence of first beam in the accelerator. This circuitry is housed in a separate 1 wide Nim module.

System Timing

In order to analyze bunch to bunch data of 2 different parameters, it is imperative that both digitizers be quantizing the same bunch simultaneously. This calls for 1 to 2 nanosecond timing constraints and delay equalization of the inputs and trigger signals.

Each of the beam processors not only has a different thru put delay, but also varying cable delays associated with beam pickups and processor location with respect to the snapshot system. Coaxial delay cables are inserted at the outputs of each processor to equalize the delay to the digitizer. (Figure 1) Likewise, a delay is added to the First Beam Trigger so that when Mth Bunch = 1; N bunches = 1; J turns = 1; and digitize gate is 0 seconds; quantizing of the first injected bunch is assured.

All clocking functions are synchronized to the low level R.F. Other arming or timing signals are obtained from the Fermilab control system.

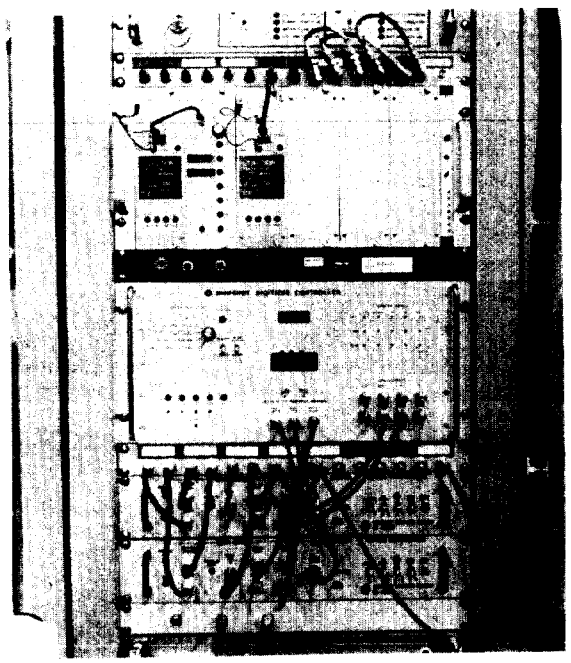

Figure 6. Snapshot Digitizer System

Performance

The system (Figure 6) is presently providing data from the RF bunch Time Discriminator, Bunch width discriminator,[1] Radial Position, and Super damper vertical position processors.[2] Data is passed on to a computer via a data interface where it is massaged and presented graphically.[3] Figure 7 shows a sample of the output in both Beam Quality mode and diagnostic mode.

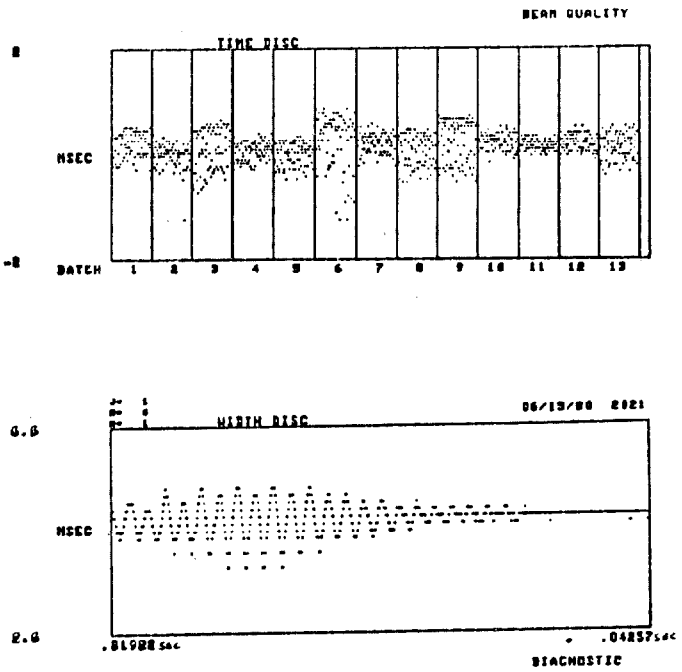

Figure 7. Performance Plots.
Top. Time Discriminator Beam Quality Mode
Bottom. Width Discriminator Diagnostic Mode

Acknowledgment

The author wishes to thank Gerry Tool for his initial guidance with the project. I also thank Peter Seifrid and Robert Hively for the skillful construction and installation of the system.

References

1. E. Higgins, C. Moore, Longitudinal Beam Signal Processing for the Fermilab Beam Quality Monitor, Paper E-36. This conference.
2. E. Higgins, Beam Signal Processing for the Fermilab Longitudinal and Transverse Beam Damping Systems, IEEE Transactions on Nuclear Science NS-22 #3, June 1975.
3. C. Moore, R. Gerig, S. Pruss, Beam Quality Measurements in Fermilab Main Ring, Paper E-15. This conference.