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THE CESR MAGNET POWER SUPPLY SYSTEM*

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Introduction

The 8 GeV electron-positron storage ring CESR[1] under construction at Cornell has the compliment of magnets listed in Table 1. The bending magnets and the interaction region quadrupole magnets are connected in series and require 990 Amps at 710 Volts for 8 GeV operation. Three 500 kW Transrex dc power supplies connected in series provide this power. The standard Transrex current control circuitry has been modified to be compatible with the control system described below. In addition, passive filters have been added to the output of the supplies to reduce the 720 Hz ripple to an acceptable level.

In order to accommodate the experimental apparatus surrounding the south interaction region a large bulge was built into the machine in that region. This breaks the symmetry of the storage ring optics and results in requiring 31 separate focal lengths for the normal lattice quadrupole magnets. For beam stability, these focal lengths must be controlled to .01%. Since there are only 90 lattice quadrupole magnets we chose to power each magnet separately and for convenience we power the sextupole and vertical and horizontal steering magnets in the same way. Two 60 volt 3000 Amp dc power supplies provide a 60 volt dc bus to power these magnets. The current through each magnet is controlled by a variable duty cycle series connected transistor switch operating at 20 kHz. This technique gives a power transfer efficiency of over 95% from the dc bus to the magnets. The set point of each magnet is controlled by either a 16-bit or 12-bit DAC which is driven by a binary scaler. By using a system of binary rate multipliers to provide the clock pulses to these scalers and driving the binary rate multipliers from a single master clock all magnets including the bending magnets can be simultaneously ramped without requiring that the magnet control computer act in real time. This control computer is a PDP 11/34 which communicates with the magnet power supplies via a bus network and control system[2] described elsewhere at this conference.

Table 1

Magnet Type	Number	I at 8 GeV (Amps)
Ring Dipole	96	990
IR Quad	8	990
Lattice Quad	90	15 - 60
Transfer Quad	10	30 - 70
Sextupole	80	0 - 40
Ring. Horz. Steer	46	± 8 max
Ring. Vert. Steer	58	± 8 max
Transf. Horz. Steer	2	± 8 max
Transf. Vert. Steer	4	± 8 max
Transf. Dipole	3	280
Transf. DC Septum	2	80 max
IR Quad Trim	4	300 max

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Magnet Control System

The magnet control computer drives a data bus servicing the east side of the ring and a data bus servicing the west side of the ring. Sixteen interface crates are distributed along each of these data buses with each crate containing a crate controller card to provide the necessary signals for the bus protocall to communicate between an interface card and the data bus. Four magnets which are normally a quadrupole, a sextupole, a vertical steering, and a horizontal steering are controlled and monitored by a magnet interface card residing in the nearest interface crate. The interface card contains the four control registers for the four 16-bit binary rate multipliers and a serial to parallel converter for reading back the 16-bit or 12-bit scaler setting which drives the DAC on the regulator card. It also contains an 8-bit ADC which reads both the magnet voltage and the error signal in the current control feedback loop for each magnet. The scaler information is stored in a 4 word by 16 bit memory with one crate address and the analog information is stored in another 4 word by 16 bit memory with another crate address. The information is automatically updated ten times per second. The data bus reads these memories to provide the computer with the present magnet operating point.

A controller crate is located near each group of four magnets (quadrupole, sextupole, vertical steering, and horizontal steering). Each magnet is controlled by a regulator card in this crate. Figure 1 is a block diagram of the magnet control system.

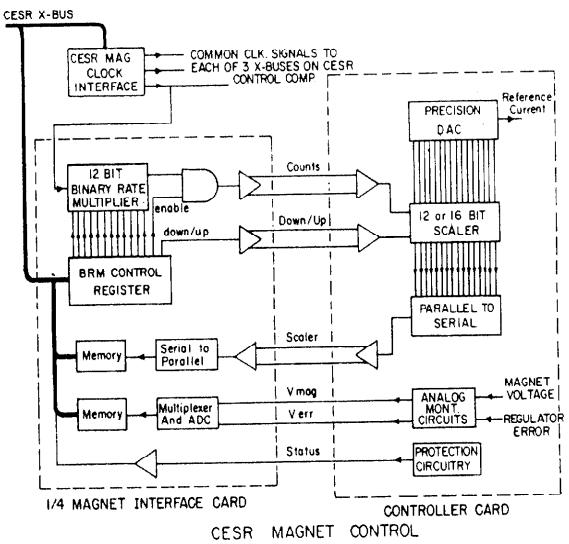

Figure 1

Quadrupole Regulator

To achieve the required .01% current regulation in the moderate noise environment of the storage ring a transductor was selected as the current monitor. An inexpensive second harmonic zero flux transductor was developed which uses a CMOS analog switch and

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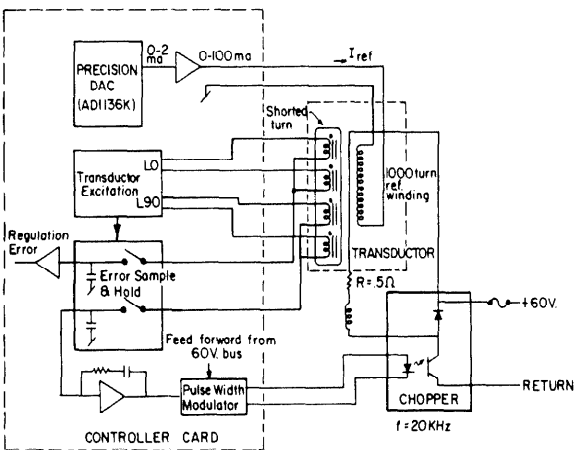
capacitor as a synchronous sample and hold to provide an error voltage directly. This eliminates the usual phase sensitive detector and current servo with a burden resistor.[3] The transductor consists of four separate magnetic cores each with ten layers of .001" x .250" Super Perm 80[4] ribbon and a 1200 turn excitation winding. These four cores are enclosed in a shorted turn, a 1000 turn bucking winding and a single coaxial turn which carries the current to be measured. The complete assembly is wrapped in oriented Si steel sheet to eliminate stray magnetic fields. The excitation windings of two cores are series connected and driven with a symmetric 10 kHz square wave with the center connection giving the error signal. A 90° phase shifted square wave drives the other two cores connected the same way with their center connection providing an independent error signal.

The regulator card contains a 16-bit DAC driven by a 16-bit scaler which counts the output of the BRM. The output of the DAC is amplified by a precision current amplifier which drives the 1000 turn bucking winding. The sample and hold and the 10 kHz square wave drives are also on the regulator card. The error signal from the transductor is proportional to the imbalance between the amp-turn in the bucking winding and the power supply current with a sensitivity of about 1 volt/1 amp-turn. The power supply current feedback control loop uses this error signal to control the pulse width modulator driving the transistor switch. The second error signal is readout by the interface card to monitor the power supply performance. Figure 2 is a block diagram of the quadrupole regulator. Because of possible variations in the bus voltage for times short compared to the 0.1 second loop resonse time a gain one voltage feed forward is included in the feedback loop. A 2% bus voltage step results in a peak excursion of less than .02% in the magnet current.



QUADRUPOLE CURRENT REGULATOR

Figure 2

The transistor switch contains four 2N6277 transistors driven in parallel by a power darlington transistor. This transistor receives its base drive from a high voltage low power switching transistor which is driven by a fast opto-isolator to avoid any low impedance ground connection to the regulator card and crate. This transistor switch has a turn on and turn off time of around 1 μsec and receives all its power from the 60 volt dc bus. A fast recovery diode is placed across the magnet to act as a free wheeling diode when the switch is off. The transistors are water cooled and provide a 100 Amp at 90% duty cycle maximum power supply rating.

A version of this system is used to power the trim windings of the interaction region quadrupoles and various elements in the beam transfer lines which has a maximum current capability of 300 amps. Five units have been constructed and operated successfully.

Sextupole and Steering Regulators

For both the sextupole magnets and steering magnets the setting accuracy is required to be only a few tenths of a percent which permits the use of a conventional shunt as the current monitor. As with the quadrupole regulators a binary rate multiplier output is scaled by a 12-bit binary scalar. This scaler then drives a 12-bit DAC which provides the control signal for the pulse width modulator driving the transistor switch. The sextupole regulator has a maximum current output of 50 Amps. The steering regulators use two transistor switches which are pulse width modulated and two transistor switches which are dc in order to reverse the polarity of the magnet. These regulators have a dynamic range of over one thousand with a maximum output current of ± 12 Amps.

System Performance

At present 250 of the 309 power supplies are installed and operating. Eighty-five of these including the five 300 Amp versions have been in regular service during the past two months of initial beam studies in the first quarter of the storage ring. There have been no in service failures of the transistor switches. The problems that have been encountered have been the usual ones of interconnection failures and initial integrated circuit failures in a system of this complexity.

As a check on several of the quadrupole regulators a precision (.01%) Leeds and Northrup shunt was placed in series with the magnet. The shunt voltage was monitored by a Fluke differential voltmeter whose output drove a strip chart recorder. The noise level in this recording system corresponded to 100 microamps through the shunt. For a typical quadrupole regulator on a lattice quadrupole operating in place at 50 amps over a 36 hour period the maximum deviation of the magnet current was less than 500 microamps. This gives current regulation to the ten part per million level.

Acknowledgements

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References

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3) H.C. Appelo, et. al., IEEE Trans. Nuc. Sci. NS-24, No. 3, 1810 (1977).

4) Super Perm 80 is manufactured by Magnetic Metals Inc. Camden, N.J.