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CURRENT TO FREQUENCY CONVERTER FOR DIGITIZATION OF MILLISECOND BEAM SIGNALS

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Summary

Beam-intensity monitoring in the Fermilab Neutrino Area requires sensitive and fast processing for beam signals (with four or five decade amplitude variations for a typcial detector) which are digitized with a current-to-frequency converter (IFC). The converter digitizes the input charge at a 1 pC/Hz rate with a processing limit at 10 MHz for a 10 nC charge input or a 10 μA current input. For a 1 ms beam pulse, the IFC can generate a 1 to 10,000 count output. The digitizer is two to three decades more sensitive than the fastest commercial V to F converters and the upper frequency limit is two or three decades higher than the present laboratory built IFC's. The resolution over the 0 to 50°C temperature range and the linearity from 1 Hz to 1 MHz is held to ± 1% with a linearity deviation of + 5% at 10 MHz.

Introduction

Several types of beam detectors are utilized in the Neutrino Area which can be monitored with the IFC. It is presently employed with ion chambers and secondary emission monitors. The output impedance of the detectors is essentially infinite and may be considered an ideal current source. Beam detector charge transfer can range over a 10^{-12}C to 10^{-3}C span. Conventional integrating amplifiers have been used successfully with the 10^{-8}C to 10^{-3}C charge range but have met with poor success in the 10^{-12}C to 10^{-9}C charge range. The IFC operates very well over the latter range and offers operation in the "real time" mode, i.e., with very little or no delay in processing fast inputs.

The conventional integrator requires several layers of system electromics before a digital quantity is available for computer digestion, whereas the IFC can interface directly to a computer-monitored scaler. The IFC output pulse train can easily be gated prior to scaling. And with two or scalers, the IFC frequency offset can be counted and subtracted from the beam-generated count, thereby neutralizing leakage and temperature-induced errors.

The IFC's processing capability for a 1 ms beam pulse offers a 1 to 10,000 count measurement. This capability while only four decades is an order-of-magnitude improvement over existing designs.

Previous laboratory efforts have yielded current-to-frequency converters with the following specifications:

Charge Sensitivity	Processing Limit	Typical Application
3 pC/count	100 kHz	SEMs with slow beam spills[1]
100 pC/count	500 kHz	long duration ion chamber counting[2]
10 pC/count	1 MHz	photomultiplier tube current monitoring[3]

Commercial voltage-to-frequency converters can be applied as positive current-to-frequency converters. Three units are very fast and can handle 1 ms pulses but lack sensitivity.

Mfg.	Model	Charge Sensitivity	Processing Limit
Philbrick	4707	200 pC/count	5 MHz
DMC	8612	200 pC/count	10 MHz
DMC	8710	100 pC/count	10 MHz

Design

The theory associated with voltage and/or current-to-frequency converters has been well covered in the literature and no further theoretical development will be offered. Schapiro[3] offers a fine analysis.

The circuit shown in Fig. 1 is a basic schematic of the IFC with the necessary device characteristics listed. The desired sensitivity is 1 pC/Hz which dictates a charge dispenser of the same value. The processing or digitizing capability necessitates an input operational amplifier with greater than a 10 MHz unity gain bandwidth product. An f_t = 20 MHz ensures that amplifier bandwidth has a minimum effect on the 10 MHz digitizing rate.

The charge dispenser pulse width should be as narrow as possible to allow a maximum output frequency. If dt is selected at 20 ns, it then follows:

$$i = Q/dt = \frac{10^{-12}\text{C}}{2 \times 10^{-8}\text{s}} = 5 \times 10^{-5}\text{A}.$$

This 50 μA discharge current and the 1 pC/Hz or 1 nA dc/Hz sensitivity dictate an input amplifier with low input bias current to minimize amplifier bias current charge of the integrating capacitor. The bias current of Al is less than 10 pA, or less than 1% of the dc current for 1 Hz operation and much less than 0.01% of the discharge current.

In order to fully realize the bandwidth of the amplifier, a very small peak-peak voltage must be generated with the charge/discharge cycle. This voltage is dependend on the value of the integrating capacitor, for C = 22 pF;

$$dV = Q/C = \frac{10^{-12}\text{C}}{22 \times 10^{-12}\text{F}} = 45\ \text{mV}.$$

It does not exceed the amplifiers slewing capability of 70 V/μs.

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The voltage ramp must also be large enough to operate the comparator. The 45 mV p-p signal is adequate for 20 MHz comparator response. Comparator-induced pulse delay is about 10 ns and is not detrimental to circuit performance.

A delay-line pulse generator follows the comparator and guarantees that the switch is driven with a 20 ns pulse width. The delay-line technique is superior to an IC monostable and RC timing circuit. The delay line exhibits excellent stability and near ideal temperature insensitivity (less than 0.01% from 0^{o} to 50^{o}C).

The single most interesting aspect of the design was the selection of the switch. For 20 ns pulse widths, the switch must have about 2 or 3 ns rise and fall times. The device chosen is a Signetics SD5000, an enhancement-type MOS transistor. The switch is a low leakage device ($\leq$ 10 nA), but is not low enough and is consequently isolated from the integrating capacitor/summing junction with diode D1. The reverse leakage current of D1 is less than 1 pA irregardless of the reverse bias voltage, which when the amplifiers bias current ($\leq$ 10 pA) is considered, ensures good low-current sensitivity without major offset current errors.

Fabrication

The basic IFC design was rather straightforward with only the design of a simple FET current source remaining. The isolation diode D1, however, presented a problem. It has a very high forward impedance when operated at 50 µA. The forward impedance varies from device to device but is approximately 20 kΩ. This is a rather large impedance to handle with a current source since the source would have to exhibit an impedance of 20 MΩ to negate diode impedance variations with temperature. The diodes forward voltage when biased at 50 µA is very sensitive to temperature changes. The voltage variation for a 20^{o}C increase is a voltage decrease of 100 mV which is larger than the expected -2 mV/C^{o} shift of most semiconductors.

The problems with the diodes impedance and temperature sensitivity were solved through the use of precision voltage source, since a temperature-compensated high-compliance current source seemed unobtainable.

Figure 2 presents the IFC or digitizer schematic in its final form with a voltage regulator U7 shown in place of the current source. The voltage regulator U7 is the classic µA723, which is flexible enough to accept a temperature-compensating circuit composed of another isolation diode and a gain setting resistor. As temperature increases and D1's forward impedance decreases, removing excess charge from C1, and in effect decreasing the output frequency; the temperature-compensating diode D2 lowers the gain of the U7 error amplifier. The output voltage follows to compensate for the lower impedance of D1. Figure 3 is a photograph of a frequency vs. temperature histogram showing the output frequency locked to within ± 0.5% over two 30^{o}C temperature excursions.

The IFC sensitivity or calibration constant is adjusted to 1 pC/Hz with the 5 kΩ potentiometer on the regulator U7. Approximately 1.5V is present at the regulator output. The circuit on the output terminal consists of a series resistor, the switch, a shunt resistor and the series isolation diode. The switch S1 has a low R_{ds}-on when handling mA sized currents, but in this circuit with only 50 µA at 1.5V to be switched the shunt resistor presents a lower impedance for the diode discharge current than another switch as in Fig. 1. Furthermore, the shunt resistor allows a forward current through S1 of 2 or 3 mA which stabilizes the R_{ds}-on for the temperature range.

The voltage pulse across the shunt resistor determines the forward diode current. Pulse amplitude is typically 0.6 to 0.8V which for a 50 µA forward current indicates a 10 k to 20 kΩ impedance.

The pulse generator circuit incorporates a unique concept for preventing over charge of the IFC. This condition must be detected, and the data so generated labeled as erroneous. Another comparator could have been tied to the output of the A1 which with the proper overload threshold adjustment would detect and indicate the overload condition. However, the additional comparator would have presented another reactive load to the input amplifier and would have reduced its frequency response. Instead, it was realized that the comparator A2 can recognize an overload condition, an indication of which is a widened output pulse. The condition is recognized with a coincidence circuit at pt. B which activates U8 and discharges C1 quickly with a wider pulse via S1 to restore normal operation.

The entire P.C.B. is sprayed with a plastic coating to prevent humidity generated leakage in the input and reset circuits. Two IFC's per P.C.B. are contained in a single-wide NIM module.

Results

The curve in Fig. 4 offers a measure of the digitizers linearity. The specified error band is ± 1% from 10 Hz or 10 pC to 1 MHz or 1 nC. At 1 MHz and above there is a distinct departure from the ± 1% band. The high frequency error is directly dependent on the frequency response of the amplifier A1 and associated stray capacitance. The f_t for the amplifier is specified at 15 MHz and in this application 20 MHz is available. The error term is a fixed fraction or percentage of the output pulse interval and is related to the frequency response as[3]

$$\tau_o \simeq \frac{1}{2\pi f_t} \simeq 8 \text{ ns.}$$

Above 1 MHz for a pulse interval of 1000 ns, approximately 1% of timing or settling time error is apparent.

This time delay error is evident in the waveform photo of Fig. 5(a). The reset or discharge time of the integrating capacitor C1 at point A in Fig. 2 is the time elapsed from the end of reset to the beginning of recharge.

The reset ramp was previously calculated to be 45 mV, but in Fig. 5(a) there is no evidence of this 45 mV ramp. However, if the time base is changed as in Fig. 5(b), the 45 mV becomes evident. The voltage excursion and excess discharge reset in Fig. 5(a) is a product of the amplifier's settling time and the stray capacitance associated with the input amplifier and comparator. The excess discharge is finally recovered when the amplifier output changes direction so that the net discharge equals 1 pC.

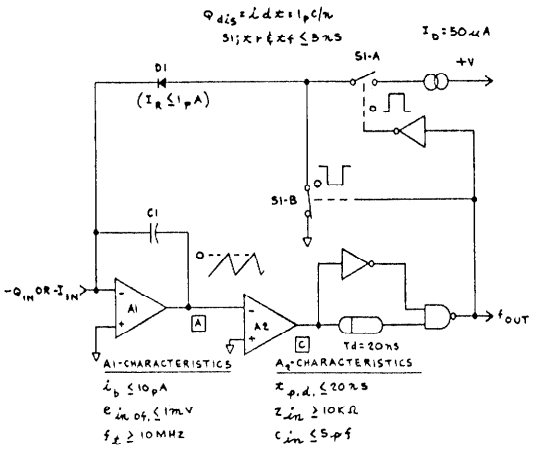

Fig. 1. Basic IFC Circuit

A capacitor discharge circuit tested the transient response. The proper charge was selected using Q = CV, selecting a capacitor, and adjusting the voltage with the discharge circuit disconnected. The capacitor was then switched into the IFC. The response to the discharge peak without an overload was 100 ns. A scaler measured the correct count and a scope displayed a pulse train with an exponential distribution of pulses in time.

Acknowledgment

IFC construction, testing, design criticism, and retesting were performed by Cecil Needles.

References

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2. R.Shafer, Fermilab Internal Report TM-391A.
3. E.G.Shapiro, IEEE Trans. Nuc. Sci. NS-17, 335(1970).

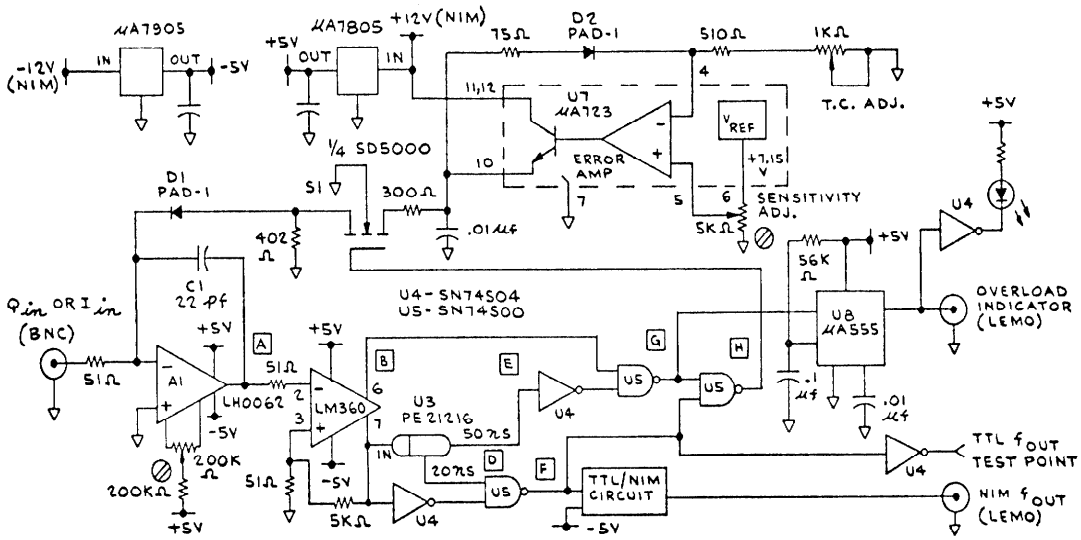

Fig. 2. Detailed IFC schematic.

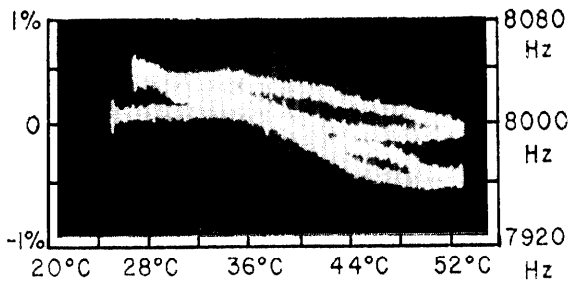

Fig. 3. IFC error vs. temperature.

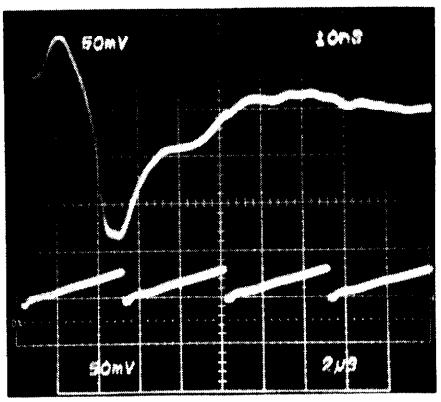

Fig. 5. Voltage waveforms at pt. A.

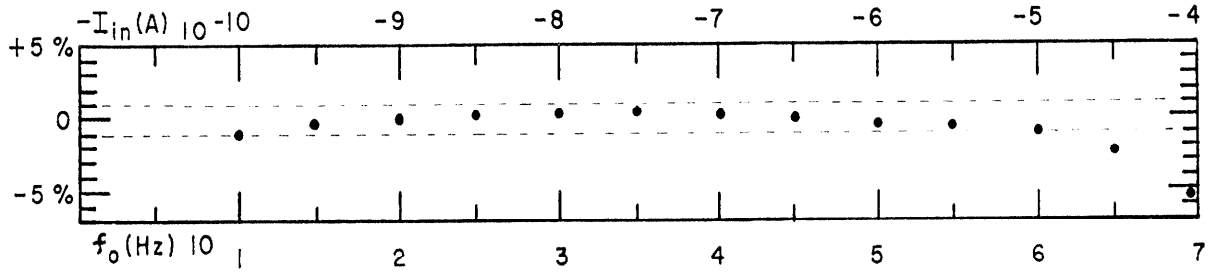

Fig. 4. Linearity vs. input current