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LOGIC AND CONTROL MODULE FOR THE FERMILAB BOOSTER BEAM DAMPER

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Introduction

A logic and control module is included in the electronic system of the booster superdamper. This module produces a 9-bit digital word that controls the delay of beam bunch position information in the Fermilab booster synchrotron so that it arrives at the damping electrodes at the same time as the bunch of beam to be corrected. This delay word generator also has an output feature that only allows delay time decreases as the booster synchrotron frequency program increases monotonically. Such a feature guards against low-index incidental FM from affecting the delay computations. The overall damper is described elsewhere.[1,2]

Delay Word Generator

The delay word generator quantizes the rf period of the booster synchrotron every 256 rf cycles. The number or word corresponding to the rf period is alternately accumulated in two binary counters called X and Y (see Fig. 1). A 119 MHz crystal-controlled oscillator is the source of these counts. Control of which counter actively counts is derived by scaling the booster frequency by 256 and using the overflow to change the state of a toggle flip-flop. The flip-flow steers the 119 MHz oscillators output to the active counter. Also, when the scaler overflows a timing sequence is initiated to synchronize the processing of the accumulated count or word in the inactive counter. The basic information is the word in the inactive X or Y counter which is proportional to the booster rf period.

Everytime a new output word is generated, an output-word-change-signal is sent to other parts of the damper. This signal prevents the beam position information and noise transients from being applied to the damping electrodes for about one beam revolution. This is done so that the 9 delay cables, controlled by the 9 bits of the output word, can clear after a cable switch. When the 119 MHz oscillator is switched from one counter to the other, there is a 0.5 probability of counting the same event in both the X and Y counters. This fact coupled with small variations in the booster frequency could result in a quantized rf period that is not monotonically shortening as the booster frequency increases from 30 to 53 MHz in its active 33 ms half-cycle.

In order to more effectively damp beam displacements, a requirement was added to the delay word generator to remove the limitations imposed by this effect. This requirement is that the 9-bit output delay word only be allowed to decrease in magnitude during the booster active half-cycle. To achieve this requirement extra processing must be done on the word in the inactive X or Y counter. This word is also selected by the toggle flip-flop to be loaded into the A multiplexed latch (A mux-latch) as soon as the last count has

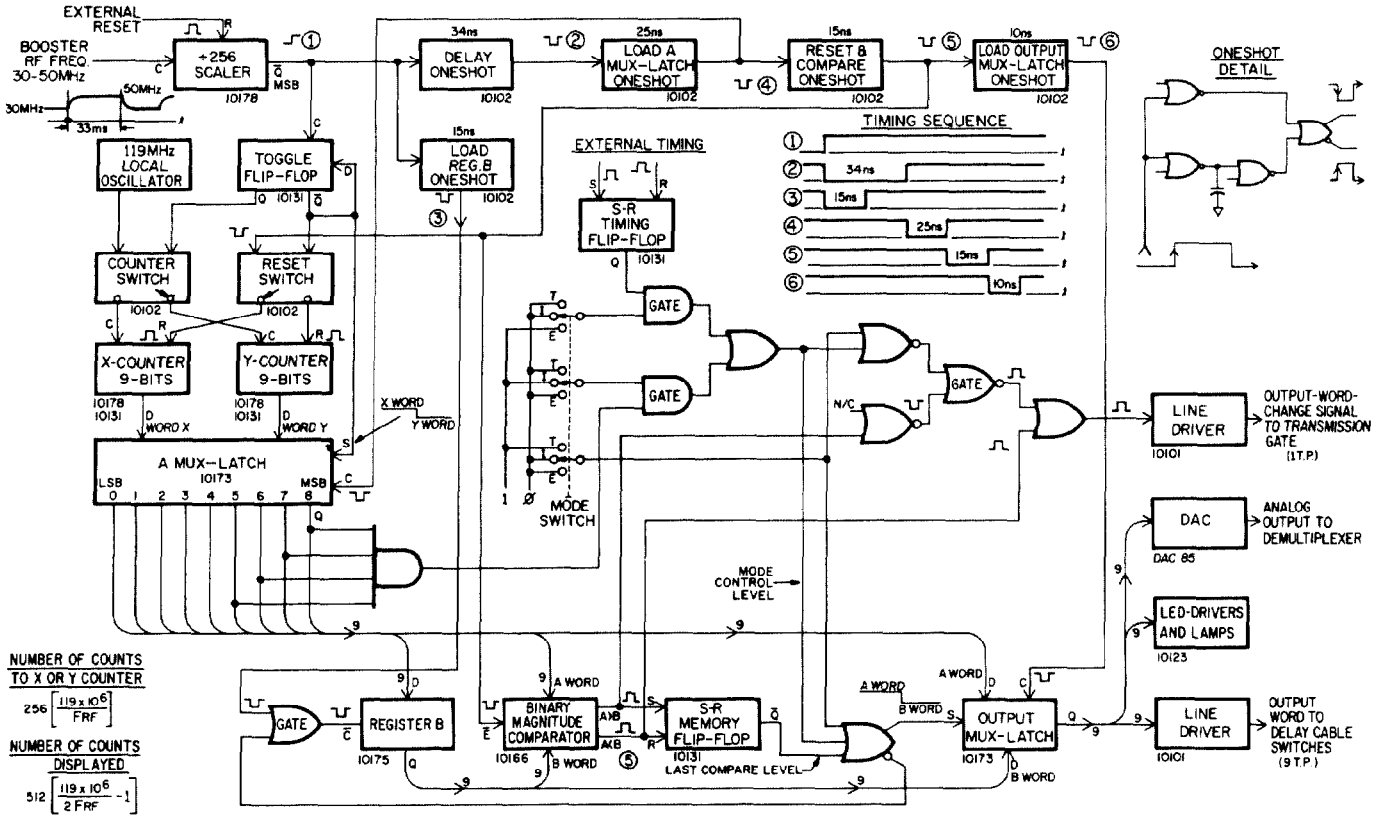

Fig. 1. Block diagram for logic and control module of booster beam damper.

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settled in the inactive X or Y counter (a 34 ns delay). Since the existing word in the A mux-latch must be saved in order to determine if the latest word settling in the X or Y counter has decreased in magnitude, the contents of the A mux-latch is usually loaded into the B register on the first phase of a four-phase timing sequence. The second phase of the timing sequence always loads the settled word in the inactive X or Y counter into the A mux-latch. With the latest word in the A mux-latch and the last valid word in the B register, the third phase of the timing sequence clears the inactive counter,

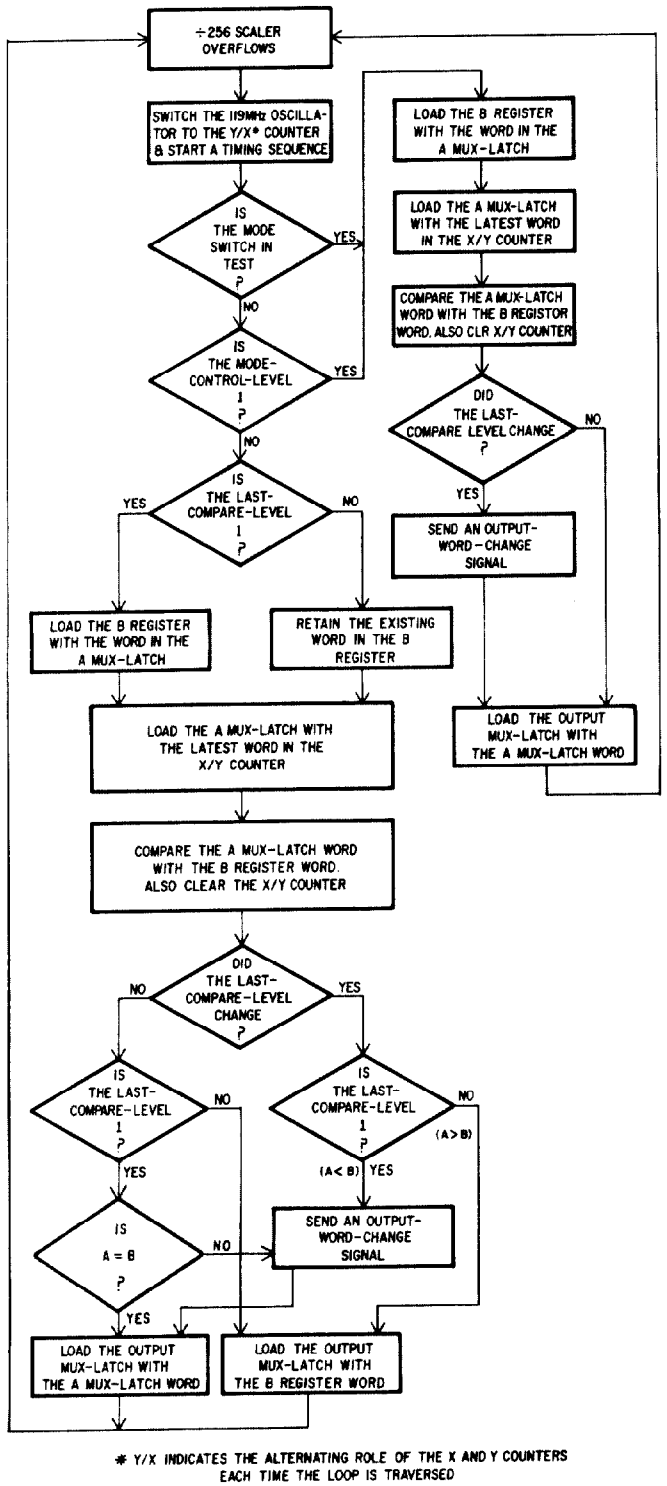

Fig. 2. Flow chart for logic and control module.

readying it to become the active counter on the next scaler overflow. The third phase also compares the words in the comparitor. The transient output of this comparator is remembered in the set-reset memory flip-flop. The $\overline{Q}$ output of the memory flip-flop is called the "last compare-level". It is high or 1 when the result of the last comparison was A<B. Finally, the fourth phase of the timing sequence loads the output mux-latch with either the A mux-latch or the B-register word depending on additional logic.

The delay word generator operates in 3 selectable modes -- test, internal and external. The test mode yields the latest word from the X or Y counter as the output word without any further processing. This mode is useful for troubleshooting the delay word generator. It is also useful for certain other digital signal processing applications. The internal mode allows the delay word generator to fulfill the decreasing magnitude requirement without external timing during most of the rf range. Below a booster frequency of 30.7 MHz as determined by the logic on the A mux-latch outputs which determines the mode control level, the output word is the same as it would be in the test mode. Between 30.7 and 53 MHz when the mode control level is low or zero, the output word is only allowed to decrease in magnitude. In the external mode, external timing signals controlling the mode control level allow the output word to initialize with the booster injection frequency of 30 MHz during the inactive booster half-cycle. Thus, the decreasing delay word requirement feature is in effect during the entire active booster half-cycle. The block diagram of Fig. 1 and the flow chart in Fig. 2 describe operation of the delay word generator better than further words would.

Construction

The delay word generator was implemented with the 10,000 ECL series of integrated circuits because of the frequencies involved. A commercial, 3-level, wire-wrap board was used for the interconnections. The 100 ohm terminating resistors to the -2 volt, middle level of the board, were enclosed in 16 pin dual in-line packages. Since the 10,000 ECL series does not include one-shots, they were made up by using logic gates as indicated in Fig. 1. These one-shots must have a zero input, prior to their circuit action, for a period longer than their timed output pulse. Thus, a cascaded chain of these one-shots must have their timed outputs decrease for each succeeding stage.

Acknowledgements

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References

[1]C. M. Ankenbrandt, E. F. Higgins, Jr., and R. Johnson; "Suppression of Transverse Instabilities by Fast Feedback in the Fermilab Booster," IEEE Trans. on Nucl. Sci., 1977 Particle Accelerator Conference Record.

[2]E. F. Higgins, Jr.; "Electronics for Damping Transverse Instabilities for Fermilab Booster Synchrotron," IEEE Trans. on Nucl. Sci., 1977 Particle Accelerator Conference Record.