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Contributed Paper

DESIGN OF A DIGITAL LOGARITHMIC RATEMETER CIRCUIT

Richard V. Osborne*

ABSTRACT

The state of a binary counter that has accumulated pulses is digitally converted to a logarithmic representation to base 2. The characteristic is determined by a shift register which locates the leading bit. A 3-bit mantissa over a factor of 2 is generated by a logic look-up table from the second to the fifth most significant bits. The root mean square error in the mantissa is 2.7% and the maximum error is 6.6%. The output signal is derived from a digital-to-analog converter. In a particular application where the analog output is displayed on a 5-decade scale for counting rates from 0.1 s^{-1} to 10^4 s^{-1}, the maximum error from conversion is less than 1% of full-scale reading. Up to 8 decades may be displayed. The minimum counts to be accumulated before conversion, and hence the statistical accuracy, may be preset. The shortest counting time is 5s but longer times, up to 640s, are automatically allowed in order to satisfy a preset count limit.

INTRODUCTION

The circuit described here has been developed for use with a monitor that measures the concentration of tritiated water vapour in the air. The tritium is collected in a stream of water which subsequently flows past a plastic scintillator[1]. For the range of concentrations monitored, pulses from the scintillator are detected at rates from a few to 10^6 per minute. One of the outputs required is the value of the concentration of activity in the sampled air on a logarithmic scale for recording and remote display.

Most logarithmic counting rate circuits are designed around multiple time constant networks driven by diodes[2] or transistors[3]. The theory of such circuits is well developed[4], but for applications needing a wide dynamic range including low counting rates such circuits present practical difficulties.

Another approach is to convert linearly a scaled count to an analog signal, using a digital-to-analog converter (DAC) and then transform the analog signal using the logarithmic characteristic obtained with diodes or diode-connected transistors. Unfortunately, for a wide dynamic range, an impracticably large bit number is required in the DAC.

However a simpler approach is possible. The logarithm of the number of counts accumulated in a given time can be derived to a given precision with only the leading digits or bits. The actual number used will depend upon the precision needed. This approach to a design for a digital logarithmic ratemeter may be resolved into three parts:

(a) Determine where the leading bits (or digits) are in the counter to obtain the characteristic of the logarithm,

(b) Extract them,

(c) Obtain a logarithmic representation, the mantissa.

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*Atomic Energy of Canada Limited
Chalk River Nuclear Laboratories
Chalk River, Ontario, K0J 1J0, Canada

Thorington and Andrews[5] selected the 2 most significant decade of a count accumulated in a 6-decade counter. The position of these decades was defined by the states of flip-flops which provided the information for deriving the characteristic and also for coding a data selector to extract the digits. A more convenient method of accomplishing parts (a) and (b) is to use the floating point compression method of Schaefer[6] as modified by Culhane and Nettleship[7]. In this method a shift register/counter accumulates the counts. At completion of the count the number of clock pulses required to shift the most significant bit to an overflow circuit is recorded in the characteristic register. The leading bits are thereby brought to a fixed position from which they may be directly extracted. The latter method also illustrates an additional advantage of binary counting over decimal counting; the rounding-off error shows less variation. If 4 bits after the leading one are extracted the maximum rounding-off error varies cyclically from 1.6% to 3.1% whereas with a 2-decade extraction (with rounding up at 4 in the third decade) the maximum error varies between 0.6% and 6%.

The final part, (c) –obtaining the mantissa from the leading bits or digits– may be accomplished by a simple look-up table or read-only memory. Iterative methods are unnecessary in this type of application. Thorington and Andrews[5], for example, converted the 8 bits of the two binary-coded decimals to a 5-bit approximation to the base-10 logarithm using logic gates, the maximum error in this 8- to 5-bit conversion being 3.6%.

The logarithmic ratemeter circuit described in this paper combines the floating point compression method (to generate the characteristic) with the look-up table method (to generate the mantissa), the digital representation of the logarithm being converted to an analog output. The logarithmic conversion is to base 2 instead of the more usual base 10. Generation of the mantissa over a factor of two rather than over a decade is more efficient and allows for simpler logic. Additionally the counting time is allowed to vary, the characteristic being adjusted accordingly. This is consistent with the property often desirable in a ratemeter, namely: that a longer counting time is associated with a low counting rate so that adequate counts can be accumulated to attain a given statistical limit. In the arrangement here, various minimum counts can be preset which must be accumulated before a logarithmic conversion can be carried out.

GENERATION OF THE LOGARITHM TO BASE 2

Because the mantissa need be derived for a factor of two rather than a decade, a given accuracy can be attained by use of fewer bits. Indeed for some purposes a quantity derived linearly from the number itself may be an adequate approximation. If the mantissa is expressed as a 3-bit number, then 8 discrete values are available over each factor of two.

Fig. 1 shows three ways of grouping the input values and assigning the groups to the 8 discrete outputs that have the values shown on the ordinate. The closest approximation to the ideal conversion (shown by the line) will be when the input values assigned to each output value span the same ratio: namely 1.0905 ($\sqrt[8]{2}$). The black bars show these assignments. For example, all input values from ~1.0443 to ~1.1388 are assigned to the output 1.0905. The maximum error (4.5%) occurs at input values close to the transition from one

output to the next. The root mean square (RMS) error is 2.5%. If the input values within each factor of 2 are divided linearly into eighths and each eighth assigned to an output value, the conversion is as shown by the open bars in Fig. 1. The maximum positive error (output scale reading high) is 7.9% and occurs at the ends of the range; the maximum negative error is -5.8% and occurs in the middle of the range. The RMS error is 2.9%. The shaded bars are the approximations derived from the 4 bits next to the leading bit in an accumulated count (i.e. the number is taken as between 1 and 2), the 16 linear divisions of the input being grouped so that the distribution on the log scale is evened out. The RMS error with this approximation is reduced to 2.7%, the maximum error to 6.6%.

For the purposes for which this ratemeter was designed, this accuracy is adequate. The mantissa is therefore derived according to the truth table shown in Table 1. The maximum errors associated with each value, i.e. the errors at the end of the bars on Fig. 1, are also given in the table. The truth table is generated by the following Boolean identities: If the accumulated number of counts is, in binary code, DCBA . . . . . then the mantissa in binary code, ZYX is given by,

$$Z = [D + B.C] \,.\, \overline{A.B.C.D}$$
$$Y = [B \oplus C + B.C.D] \,.\, \overline{A.B.C.D}$$
$$X = [(A + C + D) \,.\, \overline{B} + B.C.D] \,.\, \overline{A.B.C.D}$$

(Note that when $\overline{A.B.C.D} = 0$ then the characteristic is decremented by one less than in the other cases. The count 1111 . . . is rounded up to 10000 . . . as explained later.)

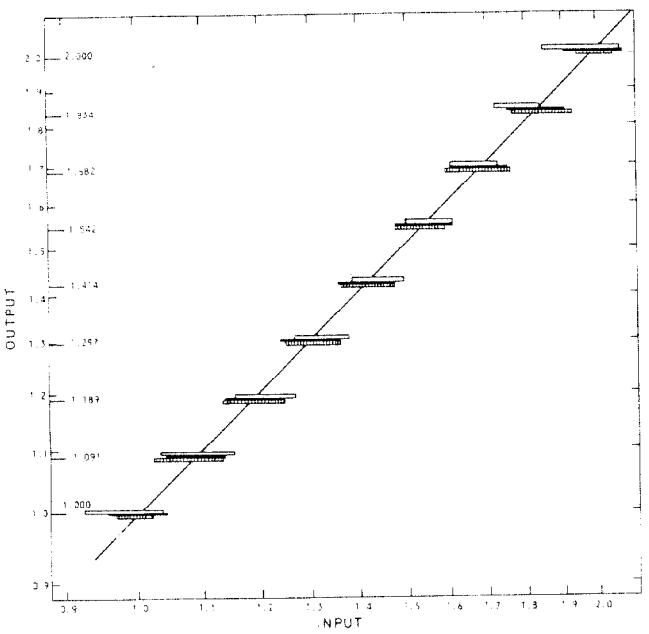

Fig. 1 – Logarithmic conversion over a factor of 2 using 3 bits. The abscissa is proportional to the input count; the ordinate is proportional to the input scale reading. The output will have one of the 8 discrete values defined by the 3 bits. Coding is as follows:

Line: ideal conversion.

Black bars: 3-bit expression, distributed so that the percentage errors are uniform over the range.

Open bars: 3-bit expression, with output a linear function of the input.

Shaded bars: 3-bit expression of mantissa derived using 4 bits of input.

In the last two sets the bars have been shifted relative to the input scales so that the estimates of the outputs are unbiased about ideal values. This corresponds to an offset at the analog output.

For 5 decades of counts, at least 17 bits are needed in the binary signal counter. The position of the leading bit and, hence, the characteristic of the logarithm to base 2 can be accommodated in a 5-bit counter. If the counting time is also to be allowed to vary from 5 s to 640 s (a factor of 2^7) then the characteristic range will be increased to 24 but this is still accommodated within the 5-bit characteristic counter. For convenience, a 20-bit signal counter has been used: the total dynamic range of counting rates which may be accomodated is therefore 2^{27}, or approximately 8 decades, with 6 decades being covered at a fixed counting time. Clearly the dynamic range may be adjusted to suit particular applications by changing the bit number in the signal, timing and characteristic counters.

With 3-bit mantissa and a 5-bit characteristic, only an 8-bit DAC is needed for the final conversion.

OUTLINE OF METHOD

The method of generating the characteristic and mantissa is shown in Fig. 2. Signal pulses are accumulated in the 20-bit binary counter and loaded in parallel into the shift register. Clock pulses are accumulated in the other binary counter. At time t (the minimum counting interval) the count-time controller receives the first stop count signal from the clock. If the pre-selected minimum count has not been attained, the characteristic is decremented by 1 from the initial preset value of 31 and the count continued. At subsequent times 2t, 4t, 8t, . . . the characteristic is decremented by 1 until the minimum count requirement is satisfied (at 2^{N-1} t say) or until the maximum counting time is reached (2^7 t). Parallel loading of the shift register is then stopped and serial shifting to the right started. At each shift step the characteristic is decremented by 1. When the leading bit reaches the overflow detector at bit 21 (after M steps say) shifting stops and the next 4 most significant bits are converted to a 3-bit logarithmic

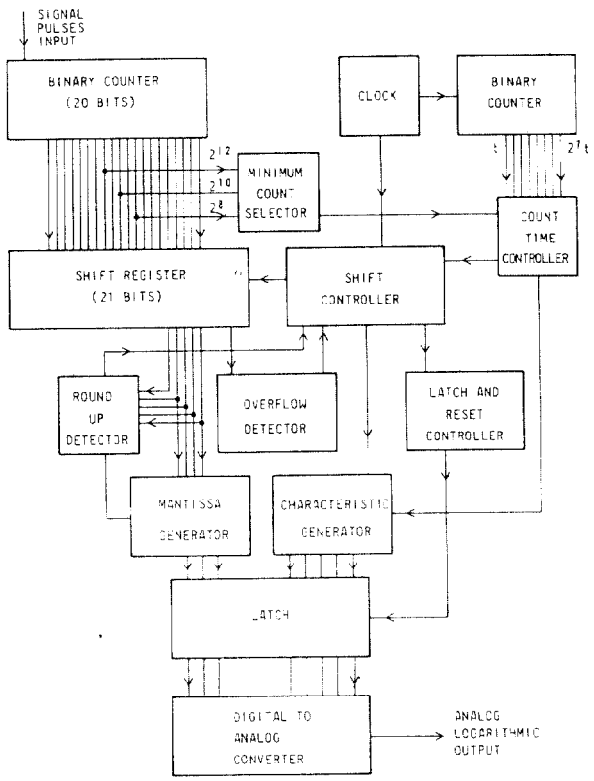

Fig. 2 – Block diagram of the digital logarithmic converter.

representation (the mantissa) as shown in Table 1. The 5-bit characteristic (31-N-M) and the 3-bit mantissa at the input to the latch are strobed to the output and hence to the digital-to-analog converter. This output is held for the next counting period which starts after reset of the counters to zero and the characteristic generator to 31.

Since N may range from 1 to 8 and M from 0 to 20 the characteristic will be between 3 and 30, i.e. between 11110 and 00011. A decade will be represented by a change in output of 11.010 or 11.011, depending upon the mantissa approximation. Table 2 illustrates the derivation of the logarithm for the arbitrarily choosen count, 467, and counts one and two decades higher. For an 8-bit DAC with 1 bit equivalent to 10V ÷ 256, a decade will be 1.035V.

MINIMUM COUNT LIMIT

Presetting of a minimum count ensures that a particular statistical accuracy is attained before the output is displayed. Since the standard deviation in the logarithmic conversion is 2.7%, there is little point in forcing a much more restrictive statistical limit: the option is therefore provided for selecting 2^8, 2^{10} or 2^{12} counts corresponding to 6.3%, 3.1% or 1.6% statistical standard deviation respectively, as well as selection of zero count limit, allowing updating of the output in the minimum time interval.

In the example taken in Table 2, if a minimum count of 2^{12} had been specified, then the count of 467 in the minimum counting interval would be carried on for 16 times this interval, giving N = 5. The count would be 7472; in binary 1110100110000, giving M = 8. The same characteristic and mantissa would therefore be generated.

TABLE 1

Input Number	Mantissa	Error* Range (%)	
0001	001	+3.5	−2.2
0010 0011	010	6.6	4.1
0100 0101	011	4.6	4.9
0110 0111	100	3.7	4.9
1000 1001	101	3.7	4.3
1010 1011	110	4.4	3.1
1100 1101 1110	111	5.7	4.5
1111 0000	000	4.1	5.1

*[(scale value ÷ input) − 1] 100%

TABLE 2

Number of Counts	Binary Counter	Time Index N	Shift Index M	Logarithm Characteristic	Logarithm Mantissa
467	111010011	1	12	10010	111
4670	1001000111110	1	8	10110	010
46700	1011011001101100	1	5	11001	100
					TO DAC

Fig. 3 shows the standard deviation of the digital output for various counting rates. With the minimum counting interval of 5s in this particular application, the abscissa corresponds to a counting rate range of $0.2\,s^{-1}$ to $2000\,s^{-1}$ With a fixed counting interval the standard deviation approaches that of the mantissa conversion (D) as the counting rate increases. Curve A illustrates this for the minimum counting interval. For clarity the root mean square error of the estimated mantissa (2.7%) has been used in deriving the total standard deviation rather than the actual error which cycles 8 times for each factor of 2 in number of counts accumulated as was shown in Fig. 1. Curve B shows the variation of the standard deviation when the minimum count limit is 2^8 counts; the deviation varies between the limits shown as the counting intervals change by factors of 2 up to the maximum of 128 times the minimum count interval. Beyond this time limit fewer counts are accumulated so that the deviation increases with decreasing counting rate. Curve C illustrates the similar variation for the minimum count limit 2^{12}.

Using the example taken in Table 2, a count of ~ 467 accumulated in the minimum counting interval would have a standard deviation of 4.6%; the overall standard deviation would be 5.4% (curve A). This counting interval would be long enough to satisfy a requirement for a minimum count of 2^8; the standard deviation with this count limit is therefore the same (curve B). With the 2^{12} limit: ~ 7472 counts would be accumulated so that the count standard deviation would be 1.2% and the overall standard deviation 2.9% (curve C).

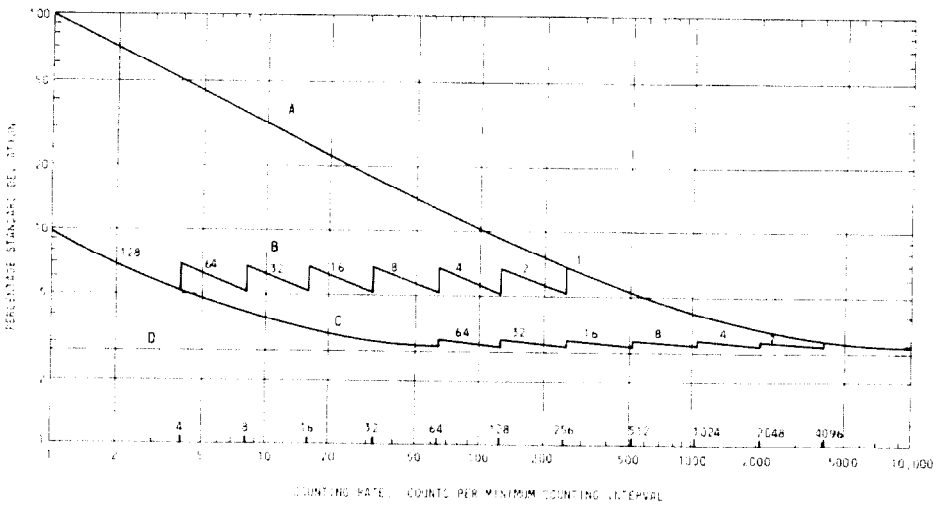

Fig. 3 – Digital logarithmic converter circuit accuracy. The combined deviations (σ) from counting statistics and the mantissa conversion are shown against counting rate. The time unit is the minimum counting interval.

Curve A: σ for minimum counting interval.

Curve B: σ for minimum counts of 2^8 within the counting interval range 1 to 128 time units.

Curve C: σ for minimum count of 2^{12} within the counting interval range 1 to 128 time units.

Curve D: average standard deviation for 3-bit mantissa only.

CIRCUIT DESCRIPTION

Counter and Mantissa Generator (Fig. 4)

The 4-bit counters accumulate the counts, and their outputs parallel-load the shift registers which are enabled by the SERIAL SHIFT signals. A low-to-high transition occurs at the MINIMUM COUNT SELECT output when the appropriate number of counts is reached. At the completion of the count the SERIAL SHIFT line goes high, parallel loading is inhibited and serial shifting enabled. The CLOCK ÷ 2 high-to-low transition shifts the count to the left and is also gated to the SHIFT INDEX output. When the leading bit reaches E of the 5-bit register, the serial shifting clock is inhibited through the NOR, NAND gates, the first monostable is triggered and the SHIFT INDEX is isolated from the CLOCK ÷ 2.

The pulse from the monostable strobes the DCBA outputs (i.e. the 2nd to the 5th leading bits) from the 5-bit register into the 4-bit latch. The second monostable is also triggered and generates the output RESET pulses to the counters, registers and flip-flop.

The SERIAL SHIFT line is high when the leading bit reaches D in the 5-bit register. Hence, if the leading bits are 11111. . . , the 6 inputs to the NAND are all high (driving the output low), serial shifting is inhibited and the first monostable is triggered. Additionally the low output sets the flip-flop which, through the NOR gate, clears the 5-bit register so that all zeros are presented to the latch. The STROBE pulse maintains the clock inhibit during this rounding up. The SHIFT INDEX makes one less transition if the shifting is terminated in this manner.

During the serial shift, ones are introduced at the serial input to the first shift register. The shift will therefore terminate after 20 steps if no counts have been accumulated during the counting interval, the leading bits being rounded up as in the previous paragraph. This has the effect of adding one count to the count converted if less than 15 counts were accumulated. Statistically, this is not important.

The MANTISSA ZYX is derived with the 9 NAND gates from the 4-bit latch outputs.

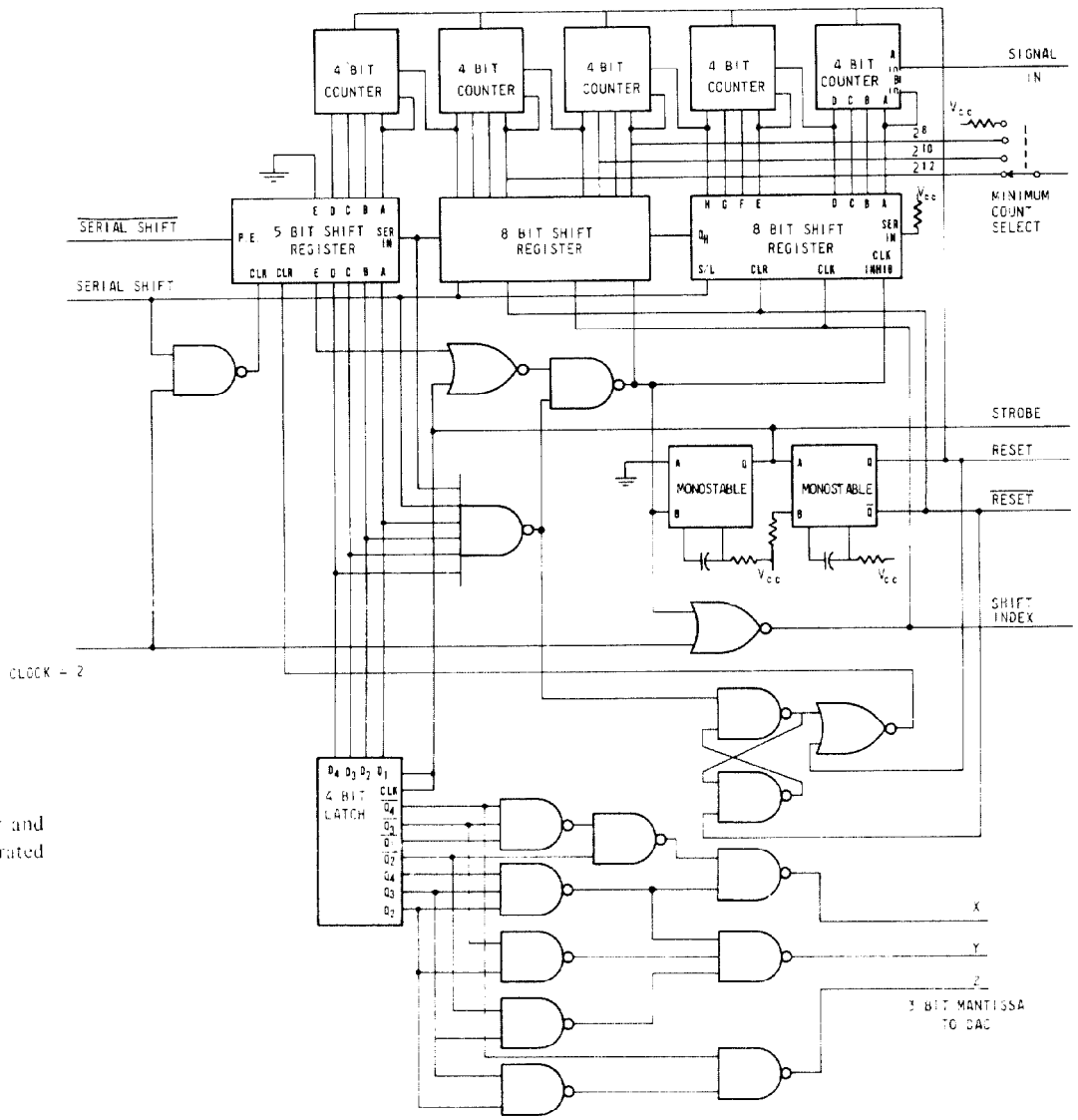

Fig. 4 Signal pulse counter and mantissa generator. The integrated circuits used are:

2-input NAND, 7400;
2-input NOR, 7402;
4-bit counter, 7493;
shift registers, 74166, 7496;
monostable, 74123;
4-bit latch, 7475;
6-input NAND, 7430;
3-input NAND, 7410.

Characteristic Generator (Fig. 5)

The clock oscillates at 409.6 Hz and provides a low-to-high transition at the 12th bit at 5 s. This signal, presented to the first input of the 8-bit data selector, is gated to the inverted output (W) since the data-select inputs (ABC) are all low. The high-to-low transition at W increments the 4-bit counter and changes the data select inputs, thereby gating the 2nd input of the selector to the output. The resultant negative-going pulse at W, the time index, is gated through to the R/S flip-flop at the right-hand side, taking the SERIAL SHIFT line high and terminating the counting period. This pulse is also gated through to the two 4-bit up/down counters set for counting down. With the SERIAL SHIFT line high, the SHIFT INDEX instead of the time index is gated to the down counter by the 3 right-hand NAND gates.

If the minimum count requirement has not been satisfied, then the MINIMUM COUNT SELECT input has not made a low-to-high transition, the left-hand side R/S flip-flop has not been set and the W pulse is prevented from enabling serial shifting. Counting therefore continues until the 10 s pulse at the 2nd input to the data selector generates a 2nd time index pulse. Counting is curtailed if the minimum count has been accumulated; if not, it continues for a total counting period of 20 s, 40 s, 80 s, etc., until the minimum count requirement is satisfied, each time index pulse decrementing the down counter.

If the minimum count has not accumulated by the time the 19th bit goes high (640 s), the minimum count flip-flop is set anyway and the time index pulse gated to the serial shift flip-flop, ending the count.

At the STROBE pulse, generated from the circuit shown in Fig. 4, the count remaining in the down counter is transferred to the 8-bit latch. The 5-bit characteristic and the 3-bit mantissa (ZYX) are presented to the input of a digital-to-analog converter.

At the RESET pulse the clock and data select counters are reset to zero and the up/down counter is set to 31 (00011111).

Rapid Update (Fig. 5)

The interval between two time index pulses increases geometrically as the count continues. To observe a sudden rise in count rate more rapidly than allowed for by the normal timing, the MINIMUM COUNT signal is scaled a factor of 4 by the independent divide-by-2 sections of the last time counter and the data select counter. When 4 times the minimum count has accumulated, the high output from the data select counter, gated at the NAND with the 12th timing counter bit, sets the serial shift flip-flop. Hence the count will terminate within 2.5 s of 4 times the minimum count being exceeded. The output will not be a time average of the counting rate during the period but a more accurate value will be rapidly obtained at the next output update, assuming that the count rate remains high.

Test

In normal operation the signal pulses are routed to the signal pulse counter as shown at the upper right hand side of Fig. 5. When the test switch is depressed the clock pulses are gated to the signal counter and the clock frequency is increased by a factor of approximately 100 by reducing the value of the controlling capacitor. Hence in 50 ms the logarithmic representation of the clock counts in this period will be

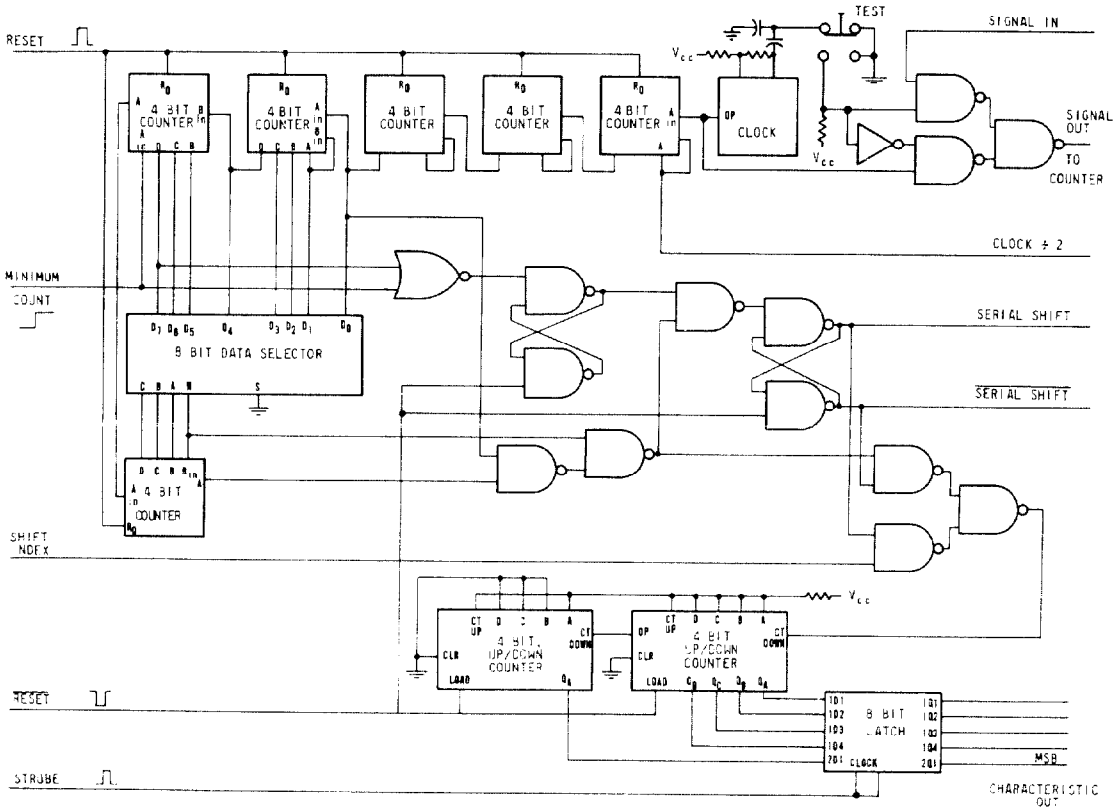

Fig. 5 Characteristic generator and test circuit. The other integrated circuits used are: 2-input NAND, 7400; 2-input NOR, 7402; 4-bit counter, 7493; 8-bit data selector 74151; 4-bit up/down counter, 74193; 8-bit latch, 74100; clock, NE555.

The timing resistors and capacitors are high stability components.

presented at the output. This will be 10101.000 irrespective of the actual clock frequency, thereby providing a check on the counting and indexing circuits but not, it should be noted, on the calibration (i.e. the output voltage from the DAC for a given input count rate).

Overall Accuracy

From Table 1 the maximum error in the logarithmic digital conversion is 6.6%. For the particular application here, 5 decades of counting rate were displayed on an analog scale; hence this maximum error corresponds to 0.6% of the full scale analog output. The variation of the clock frequency with temperature change is much smaller than this; 0.1% was measured for a 50°C change. By using a 10-bit rather than an 8-bit, DAC (Teledyne Philbrick 4023), the contribution to the error from this stage (estimated from the specification sheet) is less than 0.4% full scale for the same temperature change. Hence the maximum error in the analog output is less than 1% full scale reading which is better than most analog display devices.

Packaging and Power Consumption

The complete circuit has been built on one printed circuit board using, with the exception of the DAC, TTL integrated circuits available from several manufacturers. Fewer packages could be used and/or greater precision could be obtained by using LSI integrated circuits (e.g. a read-only memory for looking up a mantissa with more bits). However, greater precision would only be warranted if the output were to be handled digitally. Power consumption is typically 3.7W at 5V plus that of the DAC. Substitution of integrated circuits using MOS logic is possible and would, of course considerably reduce the power consumption.

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BIOGRAPHICAL SKETCH

Richard V. Osborne is a Research Officer at the Chalk River Nuclear Laboratories of Atomic Energy of Canada Limited. He was born in England and received a B.A.(Hons) in Natural Sciences from Cambridge University in 1959 and a Ph.D. in Biophysics from London University in 1962, the latter degree being obtained for research at the Institute of Cancer Research. He joined the Health Physics Branch at CRNL in 1963 where he has been concerned with the physiology of tritium and with the design and development of techniques and instruments for measuring tritium. He is a member of the Health Physics Society, Radiation Research Society, Institute of Physics and the Canadian Association of Physicists.