COMPUTER CONTROL OF THE LOS ALAMOS LINEAR ACCELERATOR*

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Summary

A data acquisition and control system for the 800-MeV proton linear accelerator for the Los Alamos Meson Physics Facility has been designed on the premise that an on-line digital computer affords the best means of maintaining operator control over the machine. The presence in the control system of a computer acting as a large programmable switching device allows the active area of the accelerator control console to be concentrated into just two panels. All information regarding the status of the accelerator, together with the capability for adjusting any control channel in the facility, is provided on these two panels. The central feature of the console is a digital CRT for alphanumeric displays. With this versatile device and the other hardware on the console, the operator will be able to execute such varied and sophisticated tasks as steering the beam down the accelerator, making phase space plots of the beam, and performing parametric studies of the effect of any control channel — all on-line. The concepts embodied in the LAMPF computer control system are being tested and evaluated in a series of experiments referred to as the Mockup Program. The status of these experiments and the associated hardware are described.

Modular Structure of the Accelerator

In order to place the computer control system for the Los Alamos Meson Physics Facility (LAMPF) in its proper perspective, it is desirable to review the design parameters and organization of the accelerator because these factors dictated to a large degree the structure of the control system.

The heart of the facility is a linear accelerator designed to produce a proton beam with an energy variable up to 800 MeV and an average current variable up to 1 mA. This proton beam is to be used primarily to produce intense secondary meson beams for the study of nuclear structure. The accelerator will pulse 120 times per second with a pulse length of 500 μsec, giving a 6% duty factor. Provisions are being made to increase the duty factor to 12% at a later date. The total length of the accelerator is approximately 2700 ft.

The distribution of power amplifiers, accelerating cavities, and various other subsystems along the length of the machine suggested that the accelerator be organized into modules and sectors. A layout of this modular grouping is shown in Fig. 1. There are a total of 55 modules in the present design. Each injector with its associated beam transport system constitutes one module. The buncher and its beam transport system make up another module. There are four modules in the low-frequency (201.25-MHz) section of the accelerator, each with one Alvarez tank. The high frequency section (805-MHz) has 45 modules with one, two, or four tanks per module. The several sector control points are grouped together to form a final module.

In designing the control system, it was natural to make use of the inherent modularity of the accelerator. This was done by establishing a centralized control point at each module. Through this control point it is possible for the accelerator operator to exercise complete control over all the subsystems comprising the module. All data required to monitor the status of the module and all signals needed to effect control over its operation are channeled through the module control point. The basic structure of the control system was established by connecting each control point to the central control area in a fan-in arrangement.

Decision for Computer Control

Having established a modular structure for the control system, there still remained the problem of organizing Central Control so that the operator could work effectively through any given module control point. The increasing availability of small digital computers specifically designed for control applications suggested that the control system be organized around an on-line computer. The arguments for and against this approach were explored in a comparative study of two possible control systems — one based on automatic sequencing hardware, the other designed around an on-line digital computer. The conclusion derived in that study[1] was that the cost of each system was approximately the same but the increased reliability and flexibility of operation plus the capability for expansion available with a computer made the computer-based control system appear much more desirable for the LAMPF installation.

There are abundant arguments supporting the contention in the last paragraph and many of them were cited at the 1965 Particle Accelerator Conference.[2] Since that time two of the arguments have become sufficiently compelling to warrant emphasis here. The first has to do with flexibility. If the computer is given access to all pertinent data sources in the accelerator and can exercise control over all operational devices in the installation, then the mode of operation of the machine is limited only by the hardware interlocks, the imagination of the operator, and the skill of

*Work performed under the auspices of the United States Atomic Energy Commission.

the programmers who write the operating programs. When the machine first goes into service, there will be many facets of its operation which will not be understood. However, as each problem is encountered and solved, the solution can be incorporated into the operating programs. As time goes on, the operator, working through a well-designed console serviced by the computer, can be expected to devise new procedures to improve the performance of the accelerator. These improvements can be incorporated in the control system without costly hardware modifications simply by modifying the operating programs. Thus the operating programs become the depository of all knowledge about the operation of the accelerator. As time goes on the computer becomes a superior operator because its memory is infallible, it performs as well at 4 in the morning as it does at 1 in the afternoon, it needs no coffee breaks or vacation, and never quits to take another job.

A second major advantage of having a computer in the control system centers around its potential for expansion. During the life of an accelerator many new control devices will be added to the installation. These additions eventually begin to strain the capacity of existing wireways or mechanical switching gear. Moreover, each new device often adds one or more panels in the control room with more lights and meters for the operator to monitor. In a digital control system the cost of adding one more bit to the channel addressing scheme so that the system can time-multiplex twice the existing number of channels is less than one percent of the original cost of the multiplexer. Moreover, the cost of doubling the memory capacity of a small computer to handle the increased data processing load is 5-10% of the cost of the computer system. Hence, the control system designer can provide for 2-3 times the anticipated maximum number of channels without perturbing the cost of the system more than a few percent. In the control room, with a computer acting as a giant programmable switching device, it is possible to concentrate the active area of the accelerator control console into a small area which the operator can readily monitor and reach. All information pertaining to the status of the accelerator and all accelerator control functions can be made available to the operator in this small area. If new data or control channels are added to the system, they can be merged into this compact control console by the console servicing programs and no additional knobs, lights, or meters are required.

Prototype Control System

Since the decision was made[3] to give computer control a full-scale test, the group at Los Alamos responsible for accelerator control has designed, built, and initiated check out of a prototype control system to provide computer control for four modules and one sector.* This effort is part of the LAMPF Mockup Program to develop, assemble, and test prototype systems for the accelerator. A layout of the operator's console as it appears in the control room is shown in Fig. 2. While this console is designed for four modules and one sector, only minor modifications are needed to provide for handling the full complement of 55 modules.

The design of the operator's console is based on a need for the operator to perform three functions: acquire data, display it, and effect changes in the data source. These three functions are essential to any control system. The data acquisition function permits the operator(s) to sense the status of the device(s) being controlled. The data must then be displayed for the operator in an easily comprehensible format. The display device can be a status light, a meter, an oscilloscope, a typewriter, or an elaborate digital CRT so long as the display conveys the information in a meaningful way. If the operator decides that the data being displayed indicate an unsatisfactory state, a link must be provided by which the operator can effect an appropriate change in the data source.

The next four sections describe the way in which the data acquisition, display, and control functions are provided in the proposed LAMPF control system with the aid of an on-line digital computer.

The Display Function

It is convenient to consider first how the requirement for a display function is fulfilled. Panel A-1 is a status panel. Binary status indicators are provided for any one of four modules. The module whose status is currently being displayed will be identified by lighting one of the four indicators on the bottom of the panel. If an operator desires to know the status of any module, he has only to press the appropriate Module Status Selector button on Panel A-3. The button will light and the computer will set the status of the selected module in the binary indicators. If the computer detects a fault or marginal operation in one of the modules, the corresponding Module Status Selector button will flash, alerting the operator to press the button and check the binary status indicators for a diagnosis of the problem. Also on panel A-1 are lamps to indicate the status of the computer and of the single sector. These are displayed continuously.

The second display device is a dual beam oscilloscope in panel A-2. The traces which appear on this oscilloscope are selectable from the Video Control area on panel A-3. With this facility, an operator can select remotely two signals from any one module or one signal from each of two modules. For example, to obtain the RF amplitude (channel 6) from module 1 as the lower trace, the operator

*Los Alamos is by no means unique in exploring the use of computers for controlling an accelerator. Note that the Proceedings of this conference contains six papers from other laboratories describing successful applications of on-line computers to the problem of controlling various portions of existing accelerators.

would dial Module 1, Channel 6, in the lower pair of thumbwheels (as shown) and press the lower Execute button. The computer would make the necessary remote connections to route the signal to the lower beam.

By far the most important and versatile display device on the control console is the digital CRT display which will be referred to hereafter as the Display Scope. This device makes it possible to display continuously (flicker-free) as many as 500 alphanumeric characters or 500 vectors or some intermediate mix of characters and vectors. Within these loose constraints, it is possible to construct a wide variety of displays.

Figure 3 shows a typical alphanumeric display providing information simultaneously on the status of Injector A and Module 1. For each channel displayed there is a 7-character channel designator, a description of the quantity being monitored, and a measured value for the channel. The value is updated typically once per second. At the bottom of the display there is room for a series of operator messages. As an example, an alarm message about a klystron is shown. This message would appear more intense than the others and could even be made to blink. In response to this message, which would also be logged on a console typewriter not shown in Fig. 2, the operator would press the corresponding Module Status Selector button to get additional information on the status panel. Also, the operator could select a diagnostic display by pressing the appropriate Display Selector button on panel B-2 of Fig. 2. These Display Selector buttons cause the computer to present some packaged display which has proved to be frequently useful, such as the display in Fig. 3. Less frequently used displays are selected with the light pen from an index of displays projected on the Display Scope.

Should an operator desire to construct a display similar to the one in Fig. 3, but with a nonstandard list of channels, he has only to dial into the thumbwheels below the Display Scope: (1) the module number, (2) the channel designator, (3) the line (Display Location) on the scope face where the display is desired, and to press the Execute button above the Display Location thumbwheels. The computer would respond by presenting a one-line display at the specified location. Repeated execution of the above steps would produce the desired display. Lines no longer wanted could be erased with the light pen.

Figure 4 is a display which is more pictorial in nature. It shows a schematic diagram of the vacuum system in the first module of the high frequency portion of the accelerator. The pressure being monitored at each ion pump is updated typically once each second. This particular display will probably evolve into a profile of the vacuum measurements down the length of the accelerator and is included primarily to indicate the capabilities of the scope.

The Control Function

The second important attribute of a control system, namely, the control function, has been implemented in the control console in at least three ways. Since no control console would be complete without a group of potentiometers so familiar in analog control systems, three slewing controls which closely approximate a potentiometer have been located in the Channel Control area on panel A-3 of Fig. 2. Their operation can be demonstrated with the aid of Fig. 5 which shows a graphical display of the beam position in both the horizontal (x) and vertical (y) directions at each point where it is measured along the accelerator. Suppose that there has been a slight but steady increase in the level of radiation monitored by one of the detectors along the accelerator. It is entirely possible for the computer to detect this trend while the radiation level is still below tolerance and flash an operator message on the Display Scope, directing the operator to call for the display in Fig. 5 by pressing the appropriate Display Selector button. The operator could see that one of the steering magnets along the accelerator needed adjusting. By dialing the module and channel number of the errant steering magnet in one set of thumbwheels under Channel Control and pressing the Up or Down (increase/decrease) button, it would be possible to steer the beam along a more desirable trajectory. The computer will effect the changes and update the display often enough for the operator to follow the effect of the correction. The Up/Down buttons provide corrections to the selected channel at a rate of 1% per second. A momentary depression of the button provides a single 0.1% change in the channel variable.

Another control area has been provided under the Display Scope. If an operator desires to set a channel to a given value, that value is dialed in the Analog Demand thumbwheels along with the module and channel numbers and the left-hand Execute button is pressed. The computer will make the desired setting. If a valve is to be opened/closed (a binary channel), the operator dials the module and channel numbers in the thumbwheels and presses On/Off to cause the computer to initiate the change provided no interlock rules are violated, in which case the OP light would come on to indicate an operator error.

A third and more powerful form of operator control has been provided with a series of Program Selector buttons. Each of these buttons causes the computer to execute a sequence of steps which may be as simple as typing out an operations log or as complex as a cold start turn-on of the accelerator. As an example of the variety of operations which can be provided by these buttons, consider the Vary program. It permits the operator to specify (probably via the console typewriter) a dependent and an independent channel (variable) together with a series of values for the independent variable. From these input data, the computer will produce on the Display Scope a graph showing the value of the dependent variable corresponding to each specified value of the

independent variable. Since a sufficient number of buttons are not provided for all the available programs, those programs used less frequently will be selected with the light pen from a program index projected on the Display Scope.

The Data Acquisition Function

The data acquisition portion of the LAMPF control system is structured as a large programmed multiplexer rather than an array of free-running multiplexers. The former is more in keeping with the concept of a computer-based control system in which the computer (or the operator through the computer) requests the data needed for the orderly operation of the facility rather than having to digest data forced on it by one or more active (free-running) sampling devices.

The LAMPF system as presently designed allows the computer to sample any of 63 possible data channels within any of the 55 modules. In addition, it is possible for the computer to sample any desired channel in all modules simultaneously or to sample a channel in all modules of a special group (e.g., all modules in a given sector). This parallelism in the data acquisition process greatly enhances the speed of the system.

Data channels are classified as binary or analog. A single binary channel can carry as many as ten binary status indications (10 bits). An analog channel corresponds to a single analog signal and the A/D conversion of the signal is carried to 0.1% (10 bits plus sign). Two types of analog signals are recognized — those which must be measured during the pulse (high frequency) and those which can be measured between pulses. If the system is taking high frequency data, sampling is performed during a reasonably stable portion of the pulse and the information stored for later transmission. Data not associated with the pulse is sampled during the beam-off period when the noise environment is assumed to be minimal. The remainder of the time between pulses is used for collection, storage, and processing of data. The times at which sampling and collection begin for both types of data are under program control.

It is anticipated that all data channels will be sampled once per second. This scanning will be initiated by the Executive program to be described later. The data scan program will sample each channel, check the measured value (or present state) against limits (or the reference state), and add the sample to the data bank. One second later, the data in the bank will be updated. Any program needing data can reference the data bank or collect fresh data. An analog channel out of limits or a binary indicator in the wrong state will cause the computer to flash an alarm message on the Display Scope (and/or type it on the console typewriter) and generate a command to return the channel to its proper value (state) if the current state of the interlocking so permits.

Design of the Control System

To understand how the LAMPF data acquisition and control system has been implemented, it is necessary to focus attention on Fig. 6. In the control room are located: (1) the control console including the CRT and video displays shown in Fig. 2, (2) the computer and its associated peripheral equipment, and (3) the CIU — Computer Interface Unit. At each module corresponding to the module control point in Fig. 1, there are (1) the RICE - Remote Information and Control Equipment, (2) the MIU - Module Interface Unit, and (3) the VCU - Video Control Unit for switching HF signals. Communications between the control room and each module control point are carried over four pairs of wires per module. This small number resulted from a decision to use serial transmission between the CIU and each RICE. The loss of speed through serial transmission was recovered by providing the capability to collect data from all modules in parallel. This design is thought to give the highest performance for the least cost and complexity. An additional two cables from each VCU back to the control console are required to carry the remotely-selected HF signals.

The control console is linked to the computer through the two 16-bit buffers. By pressing buttons and dialing thumbwheels on the console, bits are set in these buffers and a priority interrupt is sent to the computer. In response to this signal, the computer suspends its current task long enough to bring into memory the contents of the two buffers and to decode them to learn what was requested by the operator. The computer then schedules the request with the Executive program and returns to the task it was performing before the interruption. Within a few milliseconds, the computer will begin to execute the new job.

As an example, suppose the new job were a request for a profile of the RF amplitude at every high frequency module on the next pulse. The picture on the Display Scope would appear as a bar graph with the height of each bar measuring the RF amplitude at that module. To obtain the necessary data, the computer must link to the accelerator data sources. This is done through the CIU-RICE-MIU chain. The computer communicates the request for data to the CIU in the form of two 16-bit words. These bits indicate the operation to be performed (data acquisition), the modules at which data is to be collected (all high frequency modules), the channel to be sampled (RF amplitude), and how long after the start of the next pulse the sampling is to take place. The CIU transmits over two pairs of wires to each of the selected modules both the operation code and the channel address, along with a parity bit to validate the transmission. The RICE responds by connecting the selected channel (an analog signal which has been conditioned in the MIU) to the A/D converter located in each RICE.* On a signal from

*There is a significant advantage in digitizing analog data signals locally at each module as opposed to transmitting them to a central point for

(Cont'd on next page)

the CIU, the RICE converts the signal (10 bits plus sign) and stores the result in the RICE data buffer. At a later time, the computer collects the data simultaneously from all high frequency modules over the third pair of wires and stores it in specific locations in a 55-word buffer memory in the CIU. This buffer memory facilitates the collection of data simultaneously from all modules. As a final step in the process, the computer block transfers the data from the buffer memory into computer memory and signals other programs that the data is available. In this example, a display program would format the data for presentation on the Display Scope.

Acquisition of binary data is accomplished in a similar manner except that no A/D conversion is necessary. Ten binary status indicators are read simultaneously into the RICE data buffer to await collection by the computer. The time required to sample and store in the computer's memory 10 binary status indications from each of the 55 modules is less than 250 μsec.

From Fig. 6, it is evident how the display and control functions built into the control console and discussed earlier are implemented. The binary indicators on the Module Status panel are updated with binary data collected from the selected module in the way just described. Displays such as Figs. 3, 4, and 5 are generated by formatting data collected routinely or specially by the computer. A request from the operator for an oscilloscope trace goes through the computer, the CIU, and the RICE to the VCU which switches the requested video signal to one of two cables returning to the video oscilloscope on the control console.

The control functions on the console are handled in a similar way. A request from the operator for an analog set point goes via the computer and the CIU to the RICE where it is stored in a command buffer. From there, it drives a digital stepping motor through the MIU to turn a potentiometer. A request to open or close a valve follows the same route to the MIU where the appropriate relays are activated. Once the relays have responded or the potentiometer has been set, the RICE signals the computer (over the fourth pair of wires to the CIU) that the command buffer is free for another command. The computer keeps track of the status of each command buffer — busy or free.

Hybrid Nature of the Control System

From the outset of the LAMPF design effort, it was clear that there were several tasks which the computer could not perform; specifically, those tasks which required microsecond response times. For example, the computer cannot handle the fast shutdown chain. If any subsystem in the accelerator malfunctions in any way which admits the possibility of a beam spill along the accelerator, a signal must reach the injector within a few microseconds to turn it off or inhibit its operation. Present computers are not quite fast enough to respond to alarm signals on this time scale, even through the use of priority interrupts. Since protective interlocks on equipment fall into the same category as the fast shutdown chain, all safety systems and all systems related to the operational integrity of the accelerator are hardwire-interlocked. The computer is alerted to any malfunction by a priority interrupt signal and can initiate procedures to diagnose the fault and even instigate a general facility shutdown, but the initial injector inhibit signal does not proceed serially through the computer.

A second task beyond the speed capability of present computers is the fast amplitude and phase control circuit. This system must react in microseconds to compensate the RF amplitude and phase for beam loading. No small digital computer currently on the market has sufficient speed to permit it to close a servo loop having a time constant of a few microseconds. Hence, the fast amplitude and phase control loops were designed as self-contained systems which receive only their operating set point from the computer.

These two exclusions from the task list for the computer in no way detract from the capabilities of a computer control system. Rather, they emphasize that a hybrid control system — one which utilizes both wired and programmed logic — is probably the best type of control system for most accelerator installations.

LAMPF Control Computer Configuration

The remainder of this paper is devoted to a description of the hardware and software which have been developed for the prototype control system. The information is somewhat detailed and has been included to provide a clearer understanding of the design decisions made in the LAMPF control system.

Figure 7 shows the computer system as it presently exists. The central processor is an SEL-810A with 8192 16-bit words of core memory. The computer cycle time is 1.75 μsec. Parity is checked on all transfers to and from memory and the detection of an error generates an interrupt. Memory protection hardware is not essential to this application unless control functions are time-shared with debugging runs. An ASR-33 console teletype with a paper tape unit is available for programmer-computer communications.

To protect against large line transients (e.g. from lightning) and power outages, a power fail-save and restore option was obtained. If the line voltage drops below a preset value, an interrupt is generated in time to permit the computer to store the contents of volatile registers into core memory. When power is restored, a second interrupt is generated which permits the computer to restore

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sampling and conversion. A local converter is logically simpler than a central unit and the data amplifiers need not have high common mode rejection and isolation properties which tend to make them expensive.

the registers and resume where it left off.

The hardware multiply/divide option was added to the arithmetic unit to speed up conversion and calibration calculations. Floating point hardware is normally not required for a control application unless extensive numerical calculations are an integral part of the control algorithm.

A multilevel priority interrupt system is essential to any major control system. By relying on an interrupt to gain control of the central processor when a device needs attention, the computer does not have to wait for a response from the device. This is true whether the device is a typewriter or an alarm detector. Of the 30 interrupt levels purchased for this computer, 18 are used in conjunction with peripheral devices on the computer; the remainder are committed to control equipment.

Three elapsed timers were secured with the computer. The 60 c/s timer is used to maintain the time-of-day. A 20 kc counter is used for the Watchdog Timer to be discussed later. The 572 kc counter has a frequency corresponding to the computer cycle time and is used to time events within an accelerator pulse period — 8.33 ms.

To facilitate the transfer of large blocks of information to and from the computer, two block transfer channels (BTC's) were obtained to augment the standard input/output (I/O) bus structure. These channels transfer information without attention from the central processor by stealing memory cycles when the selected device is ready for service. The maximum rate of transfer of the BTC's is 572,000 words/second.

Programs are read in and punched out of the computer by means of paper tape. This mode of operation was selected over cards on the basis of space and economic considerations. Since the paper tape unit on the ASR-33 teletype is relatively slow (20 characters/s read and 10 characters/s punch), a high speed paper tape unit was added to the configuration. The reading speed of 300 characters/s is equivalent to 225 cards/min. The punch speed is 110 characters/s.

To print a lengthy log for the operator or a 500 line assembly listing for a programmer would require a prohibitively long time at the ASR-33 print speed of 10 characters/s. Hence, a line printer rated at 300 lines/min (120 characters/line) was added to the system. The line printer and high speed paper tape equipment carry the major input/output load from the computer, thereby relieving the ASR-33 of excessive use and greatly prolonging the time between failures of this device.

An additional ASR-33 was provided for the accelerator operator's use. It is needed to produce the operating log (a record of the operator's actions) and to provide a means to input and/or alter accelerator parameters. The two teletypes, together with the high speed paper tape equipment and line printer, provide the measure of redundancy needed in electromechanical I/O equipment because of its lower reliability compared to the computer mainframe.

It is not economically feasible to buy sufficient core storage to contain all programs necessary to the operation of an accelerator. Hence some sort of bulk storage device was needed. Magnetic tape equipment was ruled out because its access time is intolerable in a real-time environment. This left a choice between magnetic drums or disks. Drums generally have a faster access time but less capacity per dollar of cost when compared to disks.* The disk obtained from SEL has a capacity of 1.5 million 16-bit words on ten recording surfaces, each with its own read/write head. Since the disk spins at 2400 rpm, the arrangement of 100 tracks/surface, 16 sectors/track, and 96 words/sector makes approximately two core loadings available to the computer in a maximum of 25 ms. To move one track takes 30 ms; the seek time for the full 100 tracks is 145 ms. The transfer rate is 78,000 words/s.

The display scope shown schematically in Fig. 8 was designed to minimize the servicing load on the central processor. Hence the scope has its own memory (512 24-bit words) which is scanned automatically 60 times/s to refresh the display. Typically the display is updated once/s. However, most portions of a display do not change during its lifetime (e.g., grid lines on a graph and alphanumeric descriptions) and only a small portion of the display needs to be updated. For increased efficiency, the control unit contains both a vector generator (analog) and a character generator (5x7 dot matrix). A total of 28 μs are required to generate each vector and character. Vectors are available in two intensities. Characters are available in two sizes and two intensities. Any vector or character can be made visible to the light pen which then interrupts the computer and transmits the address of the light segment just detected.

The computer configuration described above cost approximately $200,000 and required 6 months to deliver. The central processor constituted only $40,000 of the total cost, which emphasizes the fact that 50-80% of the cost of a small computer system is in the peripheral equipment.

Interface Hardware

One of the more difficult tasks associated with a computer control system is the interfacing of equipment to be monitored and controlled. In the LAMPF system this interfacing is accomplished by a single Computer Interface Unit in the control room plus a remote unit at each module. This section is devoted to a description of these interfaces.

Figure 9 shows the prototype CIU which is composed of 4 subunits, each performing a different task in a more or less independent way. The subunits are the Word Assembler, the Memory and Block Transfer Logic, the Command Busy Register, and the Cycle Clock.

The Work Assembler portion of the CIU decodes the two 16-bit words from the computer, reassembles

*The advent of head/track disks will drastically alter this situation.

and serializes the information into the format expected by the RICE, appends a parity bit and gates the information along with concurrent timing pulses onto two lines to the selected module(s).

The Memory and Block Transfer Logic accepts data from the module(s) and performs a serial-to-parallel conversion on the data as it is being stored in unique locations in a buffer memory. Activation of the Block Transfer Channel in the computer unloads the buffer memory into the main-frame memory at the computer cycle rate of 1.75 μs/word.

The Command Busy Register maintains for each remote control unit a flag bit which is set when the computer requests the unit to execute a command. Since the remote unit may require many milliseconds to complete the command, the bit set in the busy register serves to warn the computer not to readdress the unit except in the case of priority commands. Upon completion of a command, the bit in the register is reset and the computer is alerted by an interrupt that the unit is no longer busy.

The Cycle Clock is a 16-bit counter which logs the number of computer cycles which have elapsed since the start of the accelerator pulse. It is reset by a signal from the master pulser, after which it increments every 1.75 μs until reset by the next master pulse (1/120 of a second later). The Cycle Clock can be read by the computer at any time without disturbing the contents of the counter.

The RICE contains the digital logic which performs command and data instructions under control of the CIU. An expandable input/output system (RICE I/O) collects data and performs commands under control of the RICE. The RICE I/O system is connected to the data and command instrumentation in the module through the MIU. The video control coaxial multiplexer unit is also controlled through the RICE unit. Figure 10 is a simplified block diagram of the system and Fig. 11 is a photograph of the prototype RICE and RICE I/O equipment.

The RICE unit is a synchronous digital machine consisting of a function detector, address register and decoder, instruction register, binary comparator, pulse generator and counter, data register, and control logic. Three functions are recognized by the RICE: command (CMD), data take (DTK), and video channel select (VDO). As an example of the operation of the RICE, consider the CMD function which can be either a binary output (e.g., close a relay) or an analog command (e.g., position a potentiometer). Binary commands are performed by applying each bit of the ten-bit instruction word simultaneously to its respective output. A binary comparator examines the state of each device being controlled in relation to the state requested and holds the command until a match is achieved, whereupon the command is released. Analog commands are accomplished by driving pulse motors clockwise or counterclockwise. The pulse count specified by the instruction is transferred into a pulse counter. The control logic allows this number of pulses to be routed to the addressed channel on either the clockwise or counterclockwise line. While a CMD is in execution, a signal (Command Busy) is transmitted to the CIU to notify the computer that a command is in execution.

The RICE Input/Output chassis contains the interface logic for the instrumentation and control signals between the RICE and MIU. It provides the required channel adaption and expansion flexibility to enable the RICE to be used with modules having differing numbers and types of channels. The prototype RICE I/O shown in Fig. 11 has the capacity for 32 analog inputs, 11 binary input channels (110 bits), 3 binary output channels (30 bits plus 30 latches), and 15 pulse outputs. The chassis also contains a compact, low-cost A/D converter which has a sample duration of 20 μs and a conversion speed of 10 μs/bit so that the total conversion period is on the order of 125 μs.

The MIU provides the conversion between the digital commands from the CIU-RICE system and the module equipment. In addition it conditions the binary input signals to compatible logic levels and the analog input signals to a zero to plus ten volt range.

Equipment Design

The equipment for the LAMPF prototype control system has been designed using all solid state components stressing the use of integrated circuits. The majority of the equipment employs encapsulated micrologic circuits of the type shown in Fig. 12. The notable exception to this decision has been in the module interface equipment which is fabricated in part of printed circuit cards. The printed circuit card approach was selected so that all the components for a particular command or data channel could be located on one assembly.

The encapsulated components were selected for reasons of cost, flexibility, and an existing facility for automatically wiring the connector boards for these modules. The automatic wiring of the connectors is accomplished by a wire wrapping machine which is controlled by a digital computer. Several advantages were derived using this method as opposed to the conventional man-made wire connections. First, and probably most important, the computer controlled machine does not make wiring errors and this significantly reduces check out and troubleshooting time. Second, as the wiring information appears on punched cards, an auxiliary computer program searches for missing wires and certain types of design errors. Another advantage which would be derived in mass-producing, say, 55 RICE units, is the extremely high speed with which the connections are made — 600 connections per hour.

It is too early to make any evaluation of these design choices but data are being accumulated for a review toward the end of this year.

Programming

The heart of the programming system for the LAMPF control system is EXEC, the executive program. EXEC is responsible for the allocation of all computer resources – central processor time and peripheral equipment. EXEC must also arrange for the orderly execution of all programs in core so that there are no undesirable interactions among them. The way in which EXEC accomplishes these tasks is illustrated in a superficial but informative way in Fig. 13.

EXEC maintains a list of programs called the Exec List and continually scans this list to determine whether there are programs which should be executed. There are two basic types of programs – demand and timed. A demand program is one which runs once each time it is requested either by the operator or another program. A timed program runs periodically and gets its cue from the time-of-day clock. When EXEC finds a demand program which has been demanded or a timed program which is due to run, it checks to see if the program is already in core. If so, EXEC gives control to the program by branching either to the start of the program or to a restart location if the program were already in execution but had temporarily yielded control (e.g. for an input/output operation). When a program runs to completion, it yields its core and returns control to the executive scan.

If a requested program is not already in core, EXEC checks to see if there is room for it. If there is, EXEC then arranges for the program to be brought in off the disk.* If no room is available in core, EXEC gives up for the time being and continues with the scan. Each time EXEC finishes with a program, it reloads the Watchdog Timer, a 20 kc down-counter which is typically loaded with 20,000 (equivalent to one second). If the count ever reaches zero, the WDT interrupts and gives control to the executive scan. This device insures that EXEC will regain control in the event some program gets in a tight loop or fails in some other way.

There are no priorities in the Exec List and whenever the executive scan gets control, it begins its scan where it left off previously. When it reaches the end of the list, it starts over at entry No. 1. For an Exec List with 25 entries, each program will be checked about every 1.5 ms provided there are no programs requiring any service. Programs which are used quite often (e.g., the data scan program) will have permanent slots on the Exec List. Programs used less frequently (e.g., display programs) will be assigned slots as needed on a portion of the Exec List called the Variable Exec List. In this way it is possible to have scores of programs available to EXEC.

The programming effort for essential systems programs is nearing completion. The basic system includes EXEC, all programs necessary for using the peripheral equipment plus all those to implement the operator's actions at the control console. In addition an all-channels, all-modules data scan program has been written. The Vary program described earlier and a module Turn-on program are under development. As of this writing approximately 25 man-months of labor by 5 people have gone into the programming effort over the eight months since the computer system was selected. Approximately 10,000 computer instructions are in the basic system and this implies an average productivity of 20 instructions/man-day.

*All programs are recorded in two locations on the disk. If something happens to one copy of the program, the disk subroutine tries to secure the second copy before signalling a parity error.

Summary

A comparative study of control systems indicated that a computer-based system offered LAMPF many advantages over a conventional system at essentially no extra cost. Hence, the LAMPF control system has been organized around an on-line digital computer. The three basic attributes of a control system - display, control, and data acquisition - have been implemented in a general way and the operator's console has been designed to provide for a powerful and flexible man-machine interaction. The proposed system is being tested and evaluated as part of the LAMPF mockup program in order to prove the concepts as well as develop prototype hardware and operational software.

Acknowledgments

A task having the magnitude of the LAMPF control system obviously requires the concerted efforts of a group of people. Group MP-1 at Los Alamos under the direction of T. M. Putnam is responsible for the instrumentation and control aspects of the LAMPF project. The author wishes to acknowledge the leadership of Dr. Putnam as well as individual contributions by the following people: Ezra C. Budge* - the operator's console; J. J. Smith* and Duncan Terry - the CIU; Dale Van Buren - the RICE; David Weber - the RICE I/O and VCU; J. H. Richardson - the MIU; T. M. Schultheis, J. R. Parker, and J. G. Parsons - instrumentation for the Mockup Facility; and R. F. Thomas, Jr., Dennis Simmonds, Martin D. J. MacRoberts, and Sally Ohlsen - programming. Finally, the author wishes to acknowledge the collaboration of J. J. Smith on the original system design.

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[1] Los Alamos Meson Physics Facility Control System - Preliminary Design Study Report, R. L. Hammon, Tech Report No. 675, AEC No. 1183-1069, EG&G, Inc., August 28, 1964.

[2] The Application of a Digital Computer to the Control and Monitoring of a Proton Linear Accelerator, T. M. Putnam, R. A. Jameson, and T. M. Schultheis, IEEE Transactions on Nuclear Science, Vol. NS-12, No. 3, June 1965.

[3] A Proposal for a High-Flux Meson Facility, Los Alamos Scientific Laboratory, Los Alamos, New Mexico, Sept. 1964.

*On loan from EG&G, Inc., Las Vegas, Nevada.

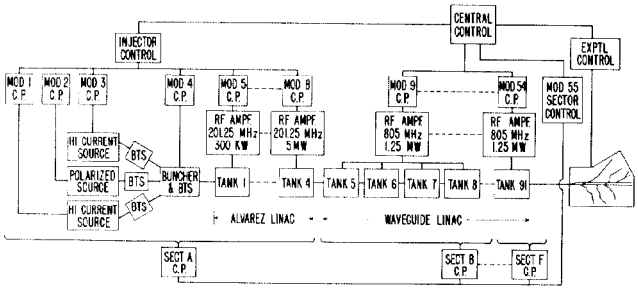

Fig. 1. Modular structure of LAMPF accelerator.

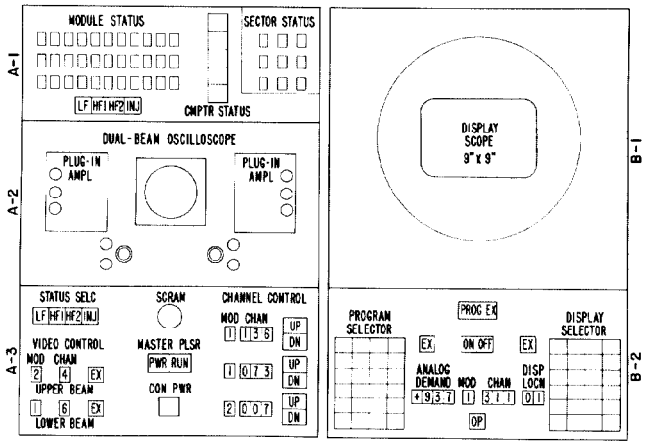

Fig. 2. Control console for the Mockup Facility. Detailed labeling has been omitted for clarity.

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                    INJ A

JA 5 23 1A  BEAM POSITION (VERTICAL)     20 MM      LOW
JA 5 23 2A  BEAM POSITION (HORIZ)         1 MM      RIGHT
JA 5 20 1A  BEAM CURRENT                4.5 MA
JA 8  1 1A  CW HI VOLTAGE               750 KV

                    MOD 1

01 2 36 1A  BEAM PHASE SHIFTER POS       70 P/C FS
01 2 31 1A  BEAM VELOCITY PHASE POS      80 P/C FS
01 7 03 1B  PA PLATE SPARK INTL             OFF
01 8 70 1B  IPA PLATE SPARK INTL            OFF
01 4 22 2A  TANK VACUUM               5.E-8 TORR
01 7 43 8B  WAVEGUIDE SPARK INTL            OFF
01 2 81 1A  DRIVE LINE SLO PH POS        24 P/C FS
01 2 88 3A  DRIVE LINE PH REF POS        30 P/C FS
01 2 61 1A  RF TANK AMPLITUDE            89 P/C FS
01 2 68 1A  RF DRIVE SLO PH POS          38 P/C FS

VDO-UP   INJ   HD VLTG
VDO-LO   HF    RF AMPL

MOD 24 KLYSTRON OPN MARGINAL
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Fig. 3. Typical alphanumeric display on the Display Scope.

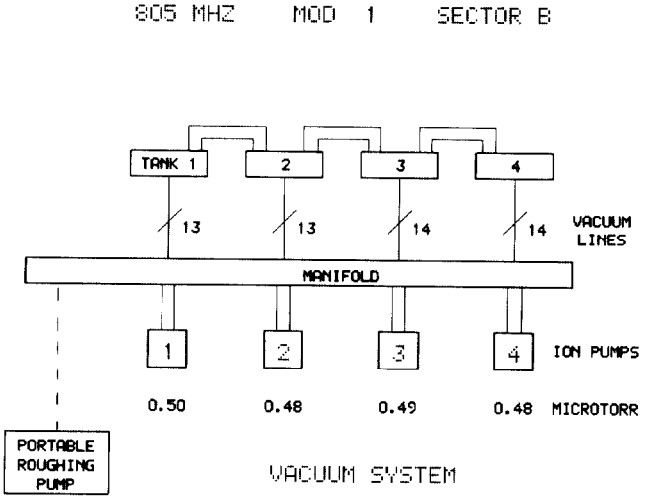

Fig. 4. Example of a pictorial display on the Display Scope.

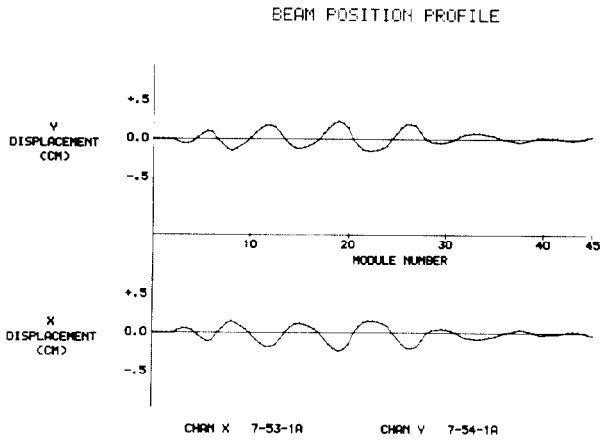

Fig. 5. Example of a graphical display which could be used to aid in steering the beam.

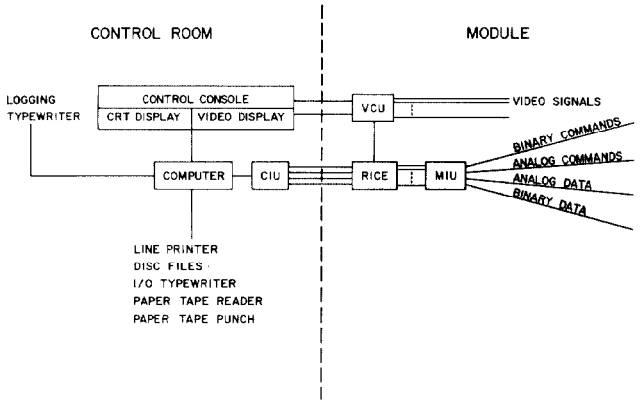

Fig. 6. Structure of LAMPF control system showing linkage between Central Control and each module control point.

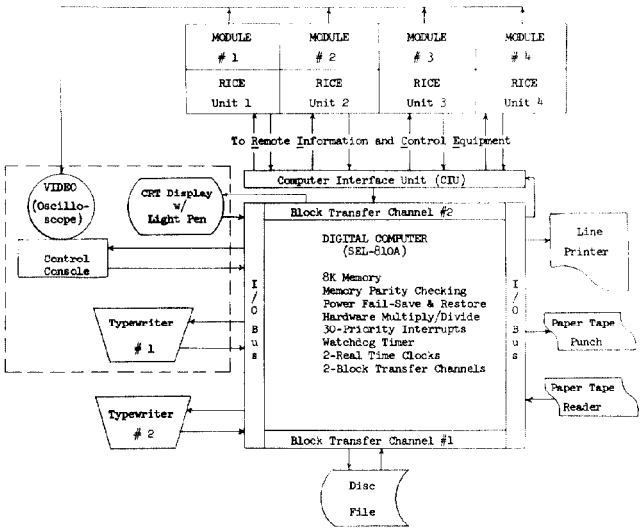

Fig. 7. Computer configuration for Mockup Facility.

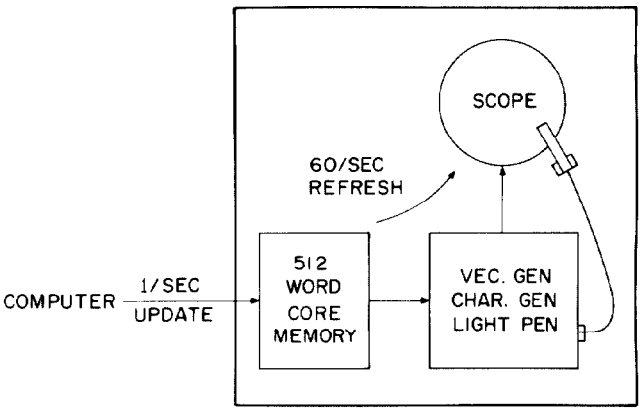

Fig. 8. Schematic of Display Scope hardware.

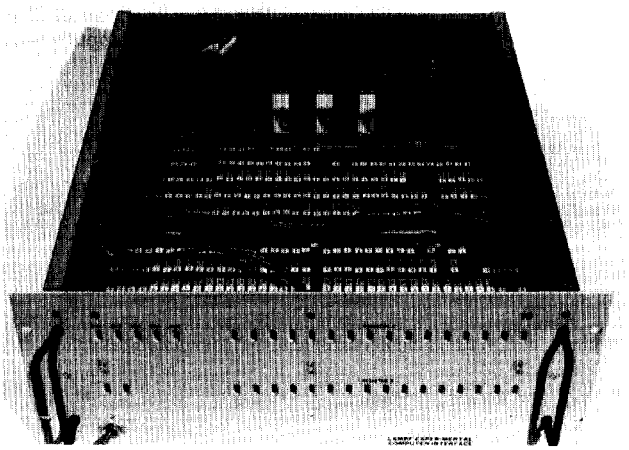

Fig. 9. Prototype of the Computer Interface Unit.

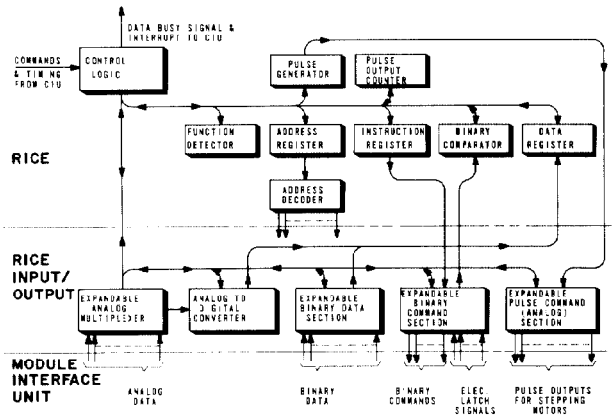

Fig. 10. Block diagram of the RICE—RICE I/0—MIU equipment.

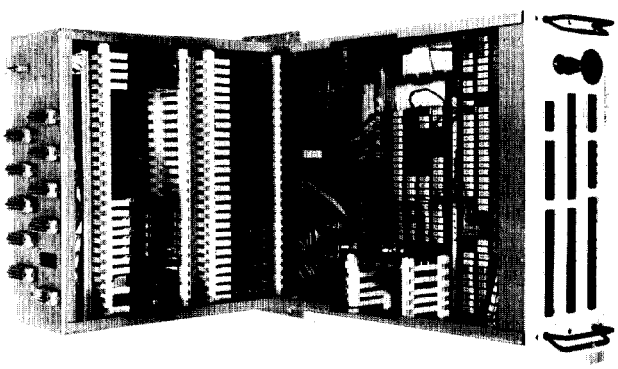

Fig. 11. Prototype of the RICE—RICE I/0 equipment.

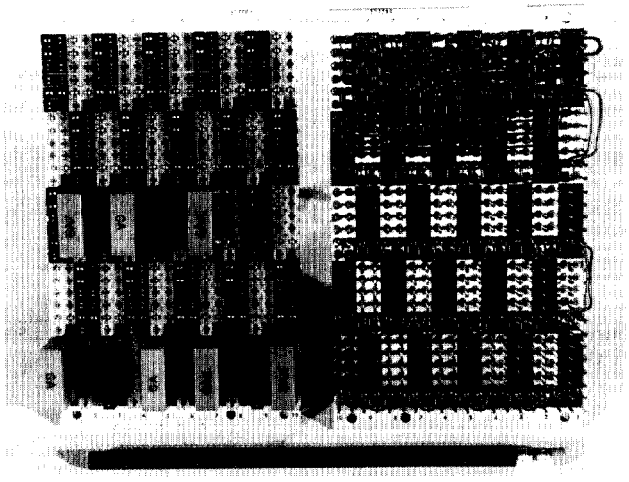

Fig. 12. Encapsulated micrologic modules mounted in computer-wired connector board.

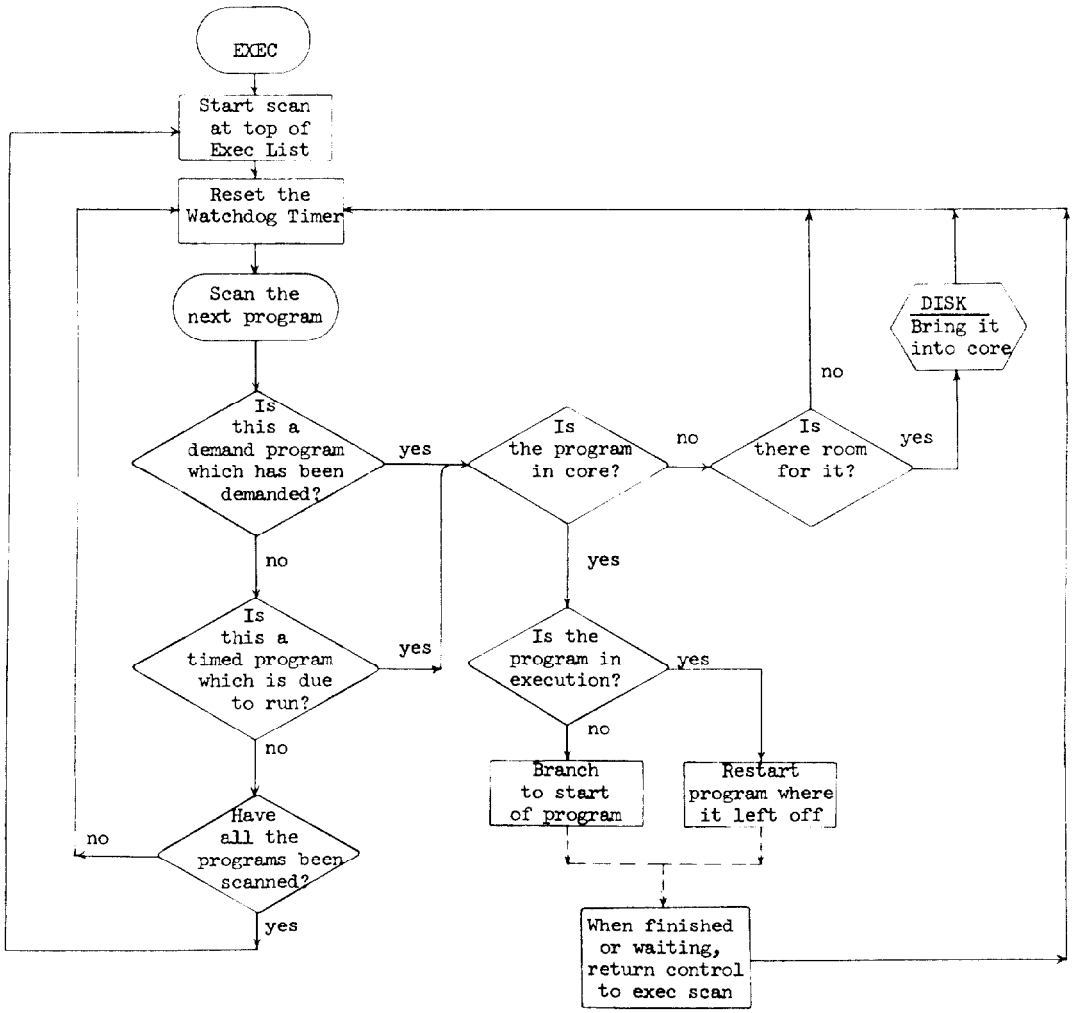

Fig. 13. Flow chart of Executive program.