# A HIGH-VOLTAGE HARD-SWITCH MODULATOR FOR THE INTERNATIONAL LINEAR COLLIDER

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*Abstract*

Diversified Technologies, Inc. (DTI) is developing a solid-state hard-switch modulator (Figure 1 and Figure 2) for the International Linear Collider, under the U.S. DOE SBIR program. This modulator will supply pulses at up to 135 kV, 165 A, and 1.5 ms for the 1.3-GHz klystrons. The full voltage is switched, so no transformer is needed.

To achieve the required pulse flatness (±0.5% at 5 Hz) without a large capacitor bank, an LC bouncer compensates for the voltage droop.

The main capacitor, which stores 92 kJ, is charged by a 185-kW DTI inverter driving a four-stage voltage multiplier. The bouncer capacitor is charged by a commercial high-voltage supply.

The main and bouncer switches are housed in an oil-filled tank, along with the inverter transformer, multiplier, bouncer inductor, and bouncer capacitor. The main capacitor bank is housed in a separate tank.

This paper describes possible modulator architectures, the design of the selected LC-bouncer, and initial testing results.

## HIGH-VOLTAGE SERIES SWITCHES

DTI has been developing switches made from series-connected IGBTs for over a decade. These switches, which have been operated at up to 160 kV, have three benefits for the ILC modulator. First, they eliminate the need for a pulse transformer – and given the voltage and pulsewidth required for ILC, any such pulse transformer will be large. Second, series switches are highly reliable because they are multiply redundant; a number of individual switches can fail (short-circuit) before the entire switch will fail. Finally, series switches provide excellent arc protection. When an arc occurs, the switch is opened, interrupting the current. No crowbar is needed – and a series switch operates faster than a crowbar. A typical DTI switch opens in <1 μs (Figure 3), while a typical crowbar requires 5 μs to extinguish an arc. Because of its faster speed, a series switch deposits an order of magnitude less energy in a fault than a crowbar, so a series switch gives substantially longer tube lifetimes.

## CANDIDATE ARCHITECTURES

The main requirements for the ILC modulator are the peak power, the ±0.5% droop, and the 1.5-ms-wide pulse. There are several possible architectures that can produce this output. The simplest is a single capacitor bank and switch. However, the capacitor bank would need to store more than 3 MJ, far more than practical.

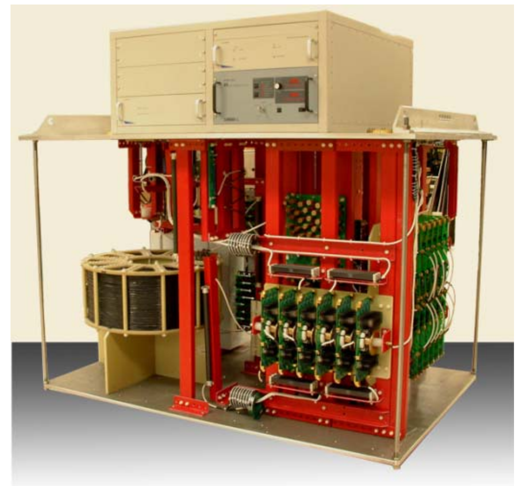

Figure 1: Photograph of the modulator. To the left is the bouncer inductor; the bouncer capacitor can be barely seen behind it. The six circuit boards in the lower right are the bouncer switches. At the far right are the main switches. The bouncer supply is mounted in the rack on top, where the control electronics will also be installed.

Instead, we chose to build a modulator with an active bouncer circuit (Figure 4). The design is similar to that of the Fermilab / DESY ILC modulator, but uses a full-voltage switch for the output, instead of a lower-voltage switch and a transformer. The capacitor bank (Figure 6) needs to store only 92 kJ. The design also requires a bouncer switch and an auxiliary power supply. The series resistance of the bouncer inductor will dissipate about 3% of the system power. (Operation of the active bouncer circuit is discussed in the next section.)

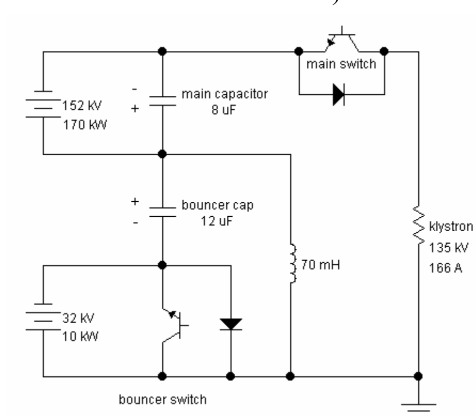


Figure 2: Simplified schematic of the hard-switch modulator. The inductor is sized such that the pulse length is about one quarter of the bouncer period.



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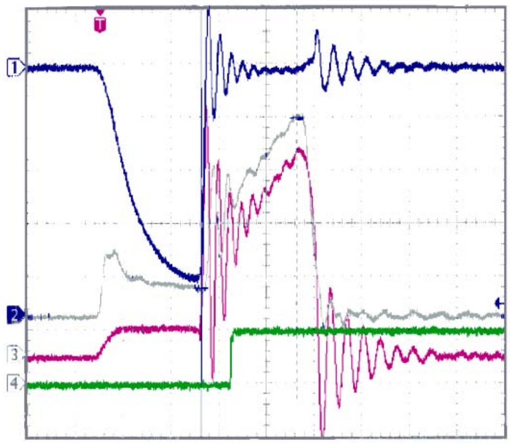

Figure 3: Opening switch arc response. Trace 1 shows cathode voltage, with the arc occurring at full voltage. Traces 2 and 3 show switch and cathode current, respectively. Trace 4 is the internal switch control. Detection of the arc, and the command for the switch to open requires ~ 200 ns from arc onset, with full switch opening in ~ 600 ns, as shown by the falling currents.

There are several other circuits that also store less energy than a simple capacitor bank. One is the passive bouncer, shown in Figure 4. This does not require an extra switch and power supply. However, the stored energy will be about 200 kJ, twice that of the active bouncer. Furthermore, the passive bouncer will dissipate 10% or more of the system power, depending on the tradeoff between the stored energy and the dissipated power. Both the stored energy and dissipation, in any combination, were deemed too large to be practical for the ILC.

A Marx bank built with opening switches is another potential candidate, since it will store 108 kJ. The Marx operates by charging the capacitors in series, then switching most of them in parallel to produce the pulsed voltage. The droop is compensated for by switching in additional modules. DTI is also building a Marx bank for ILC.

The final circuit architecture considered here is a pulse-forming network (PFN). Because the capacitors are depleted each pulse, it requires less than 60 kJ of stored energy. A PFN has the further advantages of only using a single switch and power supply. A PFN, however, requires very tight tolerances (~5%) on its components. To build a practical system would require tuning of each component, undesirable in a large system such as ILC.

## ILC HARD SWITCH MODULATOR

This modulator works in the following manner (see the schematic diagram of Figure 2 and the waveforms of Figure 5. Initially both the main and bouncer capacitors are charged by their power supplies. The bouncer switch is then closed, and the bouncer capacitor discharges through the inductor. About 1 ms later, when the voltage on the bouncer capacitor is discharging linearly, the main switch is closed.

The 31-kV voltage droop on the main capacitor is compensated for by the corresponding increase in bouncer voltage. To account for the variation in component values, the bouncer charge voltage and switch timing can be adjusted to optimize the pulse flatness.

When the output pulse is completed, the main switch opens. The current in the bouncer continues ringing, and recharges the bouncer capacitor through the bouncer diode.

### *Construction and Test Results*

DTI has built the active-bouncer modulator shown in Figure 1 and Figure 6. The inverter that drives the power supply is not shown; it is mounted in a standard 19” full-height rack.

The modulator was tested in air at 16 kV (see Figure 7 and Figure 8). The droop is compensated over the full 1.5-ms pulse; for the test here, the ripple was only ±24 V.

### *Linear Regulator*

DTI has recently proposed to add an active linear regulator to the modulator, reducing the voltage fluctuation from <1.3 kV to only a few volts in order to better achieve the ILC requirements for RF phase and amplitude stability. This linear regulator, which will have 2 kV of authority, will dissipate only 1.3 kW.

## SUMMARY

The ILC Hard Switch modulator is nearing completion at DTI, and has met its design specifications in testing to date. After the linear regulator is added, the ILC hard-switch modulator is scheduled to be installed at SLAC to test ILC multi-beam klystrons.

This hard-switch technology is being applied to both commercial accelerator systems (using a passive bouncer) and to other research accelerators. DTI recently won a contract with Rutherford Appleton Laboratory (ISIS) in the U.K. to build a modulator with very similar requirements to the ILC Hard Switch system.

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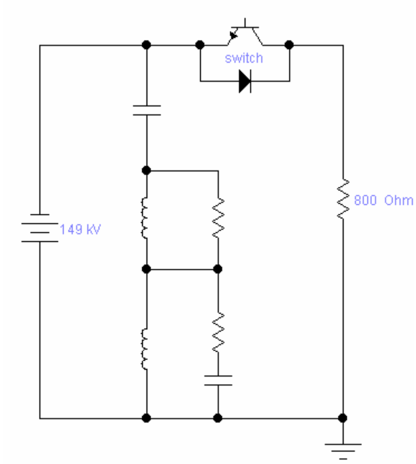


Figure 4: Passive bouncer circuit. The up LR section provides the main droop correction; the lower LRC section reduces the initial voltage spike. The stored energy and power dissipation are too large for this to be practical for ILC.

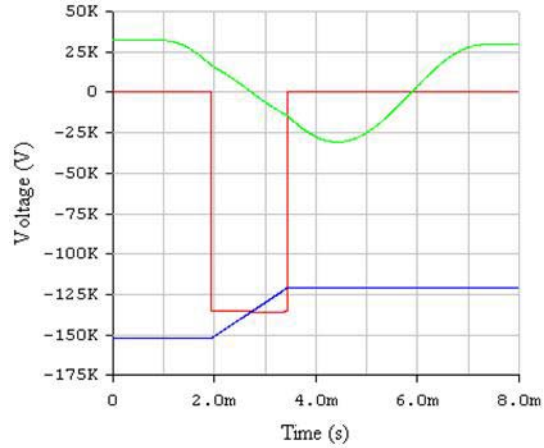


Figure 5: Voltages in the ILC hard switch. Top trace, voltage on the bouncer capacitor; bottom trace, voltage on the main capacitor; middle, combined output voltage. The bouncer circuit compensates for 31 kV of droop during the pulse.

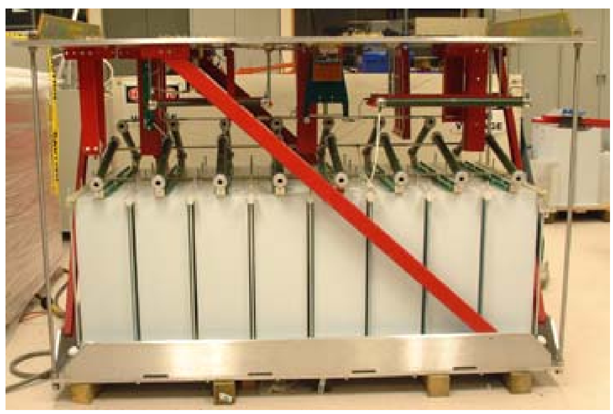

Figure 6: Capacitor bank for the ILC hard-switch modulator. The bank has a capacitance of 8 μF, a voltage of 150 kV, and stores 90 kJ.

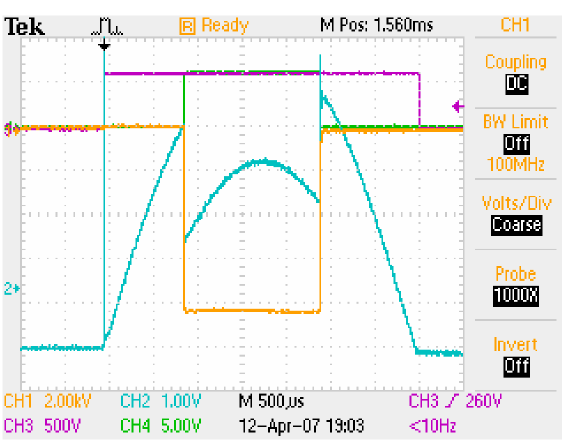


Figure 7: Test showing that the capacitor droop is compensated over the full 1.5-ms pulse. Channel 1 is the output voltage, 4 kV/div. Ch 2 is the current in bouncer capacitor, 10 A/div. Chs 3 and 4 are pulse commands.

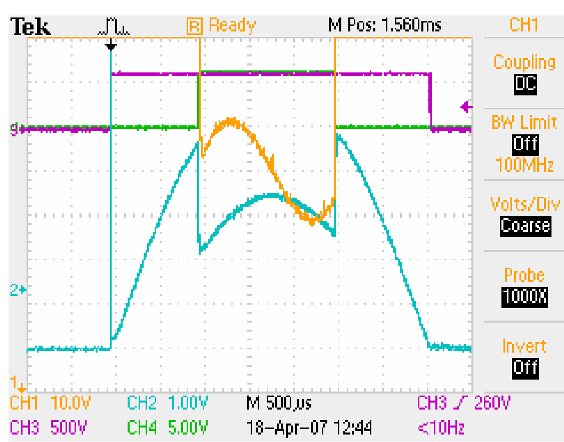


Figure 8: Test at higher sensitivity. Ch 1 is the output voltage, at 20 V/div. The ripple is ±24 V out of 16 kV, 0.15% for the conditions here.



 