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INITIAL DEVELOPMENT OF A HIGH-VOLTAGE PULSE GENERATOR FOR A SHORT-PULSE KICKER*

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Abstract

Brookhaven National Laboratory (BNL) will be the site for the Electron Ion Collider (EIC), which will require new equipment and facilities, including a 150 MeV energy recovery LINAC (ERL). The ERL requires a new short-pulse stripline kicker. The kicker requires a power system that can deliver 50 kV pulses with a width less than 38 ns into a 50 Ω load with low jitter. Inductive adders are solid-state pulsed power systems that can robustly and reliably produce short, high-voltage pulses into a variety of loads. Eagle Harbor Technologies, Inc. (EHT) has modeled, designed, and built a single stage of an inductive adder. Through experimental testing, EHT demonstrated that a single stage can meet the pulse shape, jitter, and pulse repetition frequency requirements while switching 1 kA.

INTRODUCTION

The Electron Ion Collider will enable new research in nuclear physics and quantum chromodynamics and ensure US leadership in accelerator science and technology. This upgrade will make use of existing infrastructure at Brookhaven National Laboratory (BNL) that was constructed for the Relativistic Heavy Ion Collider. However, new equipment and facilities are required, including a 150 MeV energy recovery LINAC (ERL) that will provide continuous electron beams for strong hadron cooling [1].

The ERL requires new injection kicker power systems that can produce high-voltage pulses with faster rise times. The kicker design will be qualitatively similar to the Compact Linear Collider (CLIC) damping rings' stripline kicker that consists of two parallel electrodes housed inside a conducting cylinder. Each electrode is charged by an equal, but opposite polarity, high-voltage pulse [2-3].

The CLIC kicker power supply needed to produce ±12.5 kV pulses into 50 Ω loads (250 A). The 160 ns flat-top could deviate by no more than ±0.02% (±2.5 V) combined droop and ripple. The rise was less challenging (< 250 ns). The required pulse repetition frequency was 50 Hz [4].

The BNL kickers require higher voltage and shorter pulse widths. At that start of the Phase I program, the specifications for the ERL kickers were as follows:

- Output voltage: ±50 kV ±2% for flattop
- Output current: 1 kA
- Load impedance: 50 Ω
- Pulse shape: 6 ns rise, 20 ns flattop, 12 ns fall (with residual voltage below 1 kV after 38 ns)
- Pulse repetition frequency: 10 Hz (during operation) and 100 Hz (lifetime testing)
- Robust to faults (short/open/noise)
- High reliability: Operate 12–20 weeks out of the year (availability 99% or better)
- Jitter < 0.5 ns with respect to external clock

INDUCTIVE ADDERS

The CLIC kicker power system used an inductive adder topology. An inductive adder consists of N printed circuit boards (PCBs) that contain a solid-state switch, energy storage capacitor, and the primary winding of a transformer. The transformer primaries are connected in parallel, and their secondaries are connected in series. A four-stage inductive adder is shown in Fig. 1 with stray inductance on each primary stage. The gray toroids are the transformer cores. The transformer secondary consists of a central rod connected to ground on one end and the metal cylinder that goes around the outside of the transformer cores. The load is connected between the two or at the end of a transmission line.

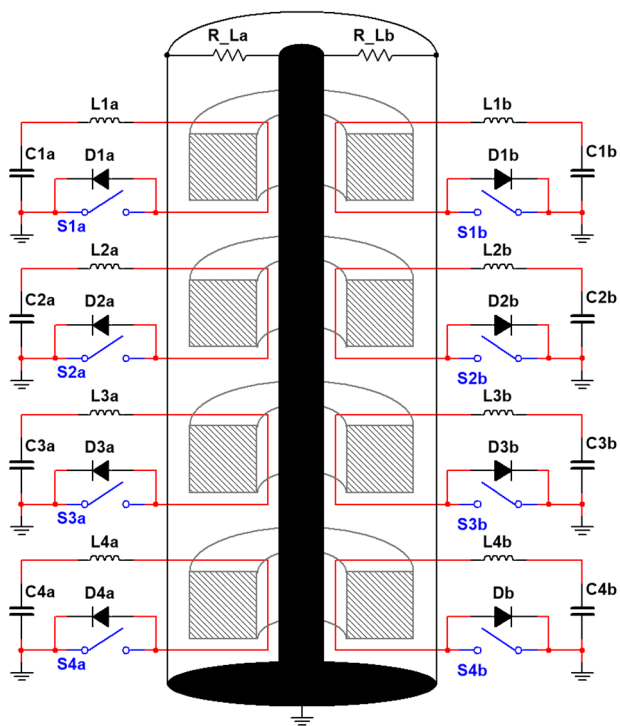

Figure 1: Four-stage inductive adder. The image is symmetric about the central stack.

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Inductive adders have several features that make them advantageous over other modulator options:

- Limit the presence of high voltage to the transformer. All circuit components operate < 1 kV.
- Solid-state switches (e.g., SiC MOSFETs and IGBTs) allow for user-adjustable pulse widths.
- Operation at < 1 kHz requires no additional R&D because of solid-state switches.
- Off-the-shelf components are used. When newer components become available, these can be replaced to improve performance of future systems.
- All components are used within manufacturers' specifications, leading to long system lifetimes.
- Single-stage failure does not fail the power system.

EHT is developing a 50 kV inductive adder that can meet the BNL pulse shape specifications. Here we present the development of a single stage of the inductive adder.

CIRCUIT MODELING

EHT previously developed a SPICE model when designing a 20 kV inductive adder. This single-stage model was updated (Fig. 2) and used to evaluate what design changes are needed to improve the pulse timing and meet the flattop requirements. The single-stage model used a 1.56 Ω load, requiring 1 kA. In the full 50 kV stack, 32 stages will be required.

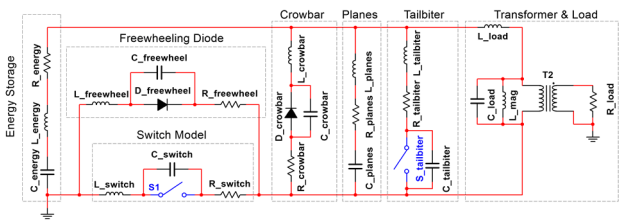

Figure 2: Single-stage inductive adder SPICE model circuit diagram with addition of a tailbiter circuit.

To reduce the fall time, EHT added a tailbiter circuit, which is a switch in parallel with the load. This switch is closed at the end of a pulse to rapidly discharge the load and plane capacitances, allowing the main switch capacitance to recharge more quickly. A small resistance was added to the tailbiter to allow adjustability of the RC time constant, limit the current in the tailbiter switches, and damp out the ringing. Based on the inductance and capacitance calculations, one tailbiter switch per main switch is sufficient.

During this modeling, EHT identified four key approaches to improving performance: reducing plane capacitance, using new switches with a smaller footprint and lower capacitance, adding a tailbiter circuit, and decreasing the output inductance. Fig. 3 shows the SPICE model output waveform measured into a 1.56 Ω load. This single-stage waveform meets the challenging timing specifications required by BNL.

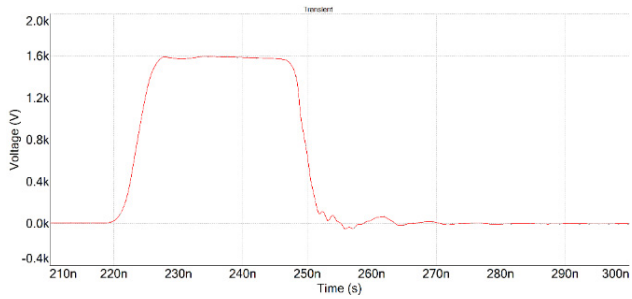

Figure 3: Output waveform of SPICE model with new switches for both the main switch and tailbiter.

PRINTED CIRCUIT BOARD DESIGN

Using these modeling results to guide the PCB design, EHT designed a new inductive adder PCB that utilized new switches, added a tailbiter circuit, and decreased the stray plane capacitance. The smaller TO-263-7 package allowed us to continue using 96 main switches (same as the previous unit) while adding 48 tailbiter switches on the same size PCB. Fig. 4 shows a side-by-side comparison of the previous and new PCB designs.

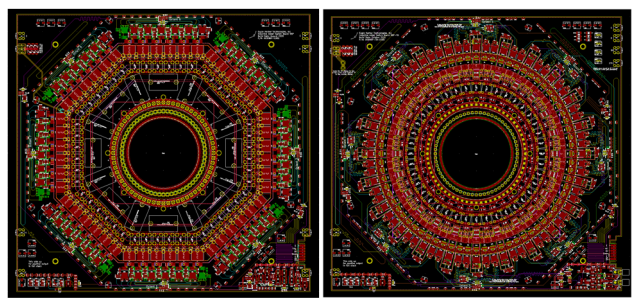

Figure 4: Comparison of the original (left) and BNL Phase I (right) PCBs. Both boards have the same dimensions.

The tailbiter switches require independent drive circuitry, which complicates the PCB design. A digital isolator for the drive signal and isolated power planes for the tailbiter circuit are required to float the switch and gate because the source pins cannot be tied to ground. The smaller package of the new switch provided space for the additional isolated circuitry to fit on the PCB.

The new inductive adder PCB also has a lower plane capacitance. Two factors contributed to reducing the plane area: the smaller switch package and a circular switch arrangement instead of an octagonal arrangement like the previous IA design. The smaller switch footprint necessitates a smaller area of copper beneath it, and in turn decreases the overall area of the top and bottom copper planes that the switches are populated on.

The circular arrangement is a more efficient use of space than an octagonal arrangement. The switches were moved radially inward on the PCB and populated more densely, resulting in a smaller area of copper planes that are connected to the switches. The gate drive circuitry was placed radially outward from switches. If the switches were populated more densely in an octagonal arrangement, the drive circuitry would need to fan out in a non-symmetric pattern to fit all the necessary components. This would result in

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different gate trace lengths for each switch in an octagon. The circular arrangement was the best way to reduce the area of the fluctuating planes and keep a symmetric pattern for the drive circuitry on the entire board.

WAVEFORM DEMONSTRATION

For testing, a jig connects the PCB under test to a low-inductance load in a coaxial arrangement that mimics the per-board impedance of the full inductive adder stack (Fig. 5). The test jig was 3D printed with PETG plastic and wrapped with copper tape to conduct from the PCB to the load. The load PCB sits atop the 3D-printed parts and contains three sets of 64 parallel MELF resistors in series. The load is 1.56 Ω, requiring 1 kA for the single-board test.

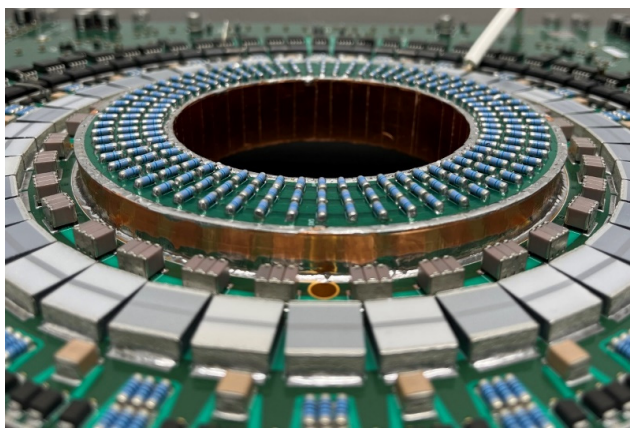

Figure 5: 3D printed low-inductance test jig for installed on the inductive adder PCB.

Figure 6 is an example waveform from the PCB at full charge voltage that was gathered with a Tektronix IsoVu probe. This waveform shows that the flat top stability is within ±2%. The voltage rise and fall times are defined from 2–98%. While switching the full current (1 kA), the waveform has a 20 ns flat top and 38 ns pulse width. The rise time and fall time are approximately 8 and 10 ns respectively. The flat top is adjustable by a few nanoseconds.

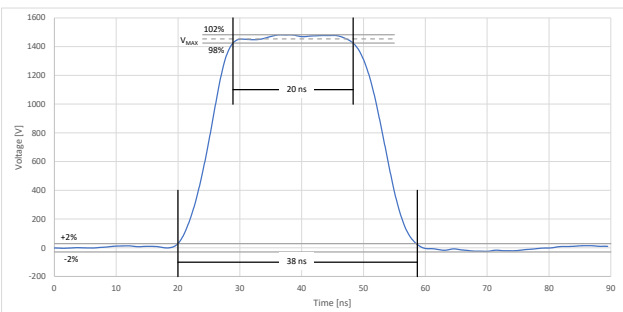

Figure 6: Waveform at full voltage and full current. Annotated with horizontal bars to denote the ±2% of maximum voltage and a ±2% window around the maximum voltage. Also annotated with vertical bars to denote a 20 ns flat top length and 38 ns overall pulse length.

In addition to the pulse shape specifications, demonstrating a jitter below 500 ps was required. From previous work, the fiber component is the largest source of jitter and will not be used in the full stack constructed in a potential Phase II program. To remove the jitter effects from the fiber component, we measured the delay between the signal input's first logic chip and the HV output and created a histogram. Data on 200 consecutive pulses were collected for the histogram (Fig. 7). The absolute range of delay is merely 350 ps with a standard deviation of 43 ps. Thus, jitter of the system is much smaller than the specified 500 ps by all measures.

Figure 7: Measuring the delay from the board signal input and board output. The top histogram was created by the Tektronix scope and data exported to Excel for further processing.

The last test was continuous operation at 100 Hz and 500 Hz for several minutes. Performance was consistent for the full duration, and IR camera measurements indicated that no components were heating significantly. Because of the lack of heating, the board can operate at 100 Hz for long durations. Higher-frequency operation was limited by the low-voltage power regulators which will not be on the full stack. The full stack will easily be able to operate above 1 kHz, which will allow for efficient lifetime testing.

CONCLUSION

EHT successfully modeled, designed, built, and tested a single-stage inductive adder PCB. During the testing phase, EHT demonstrated that this single stage can meet the challenging timing specifications outlined by BNL, including low-jitter operation. Additionally, this system can operate at frequencies above 1 kHz, though that is not required for BNL. The next stage of this program is to finish designing the 32-stage inductive adder that will be able to produce 50 kV into 50 Ω. Afterwards, EHT will build and test this inductive adder.

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